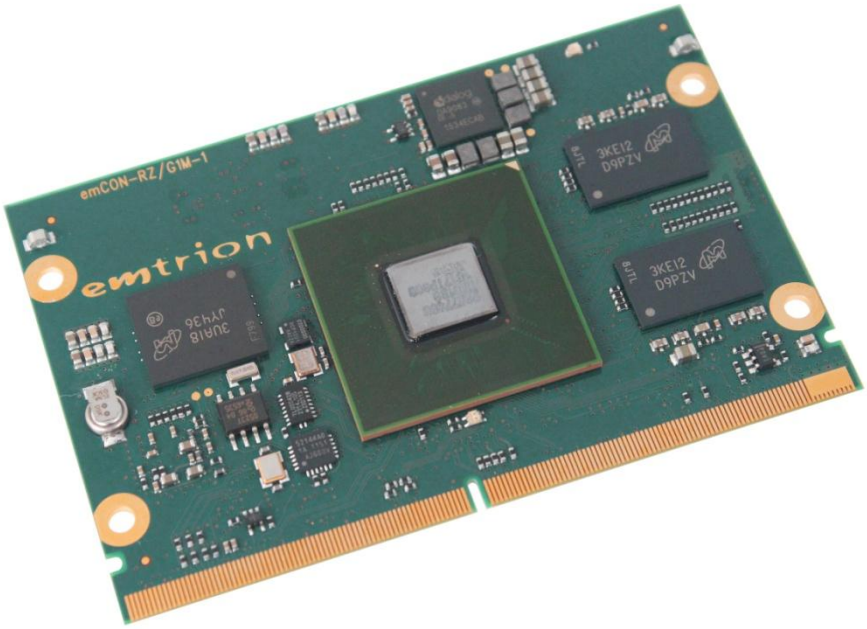
emCON-RZ/G1C - Hardware Manual

Hardware Manual

V2 / 22.08.2019



emtrion GmbH

Revision: **V2 / 22.08.2019**

Rev	Date/Signature	Changes
1	30.10.17/Bue	First release
2	22.08.19/Bue	GPIOs at emCON connector in chapter 6.1 corrected

Contents

1 Introduction

The emCON-RZ/G1C module is a CPU board of emtrion's emCON-family based on the RZ/G1C processor from Renesas.

The RZ/G1C features basic functions for general-purpose and Rich Graphics applications. It is equipped with dual-core Cortex™-A7. The cores are accompanied by a variety of functions required for graphics and industrial applications. These functions include a 3D graphics accelerator, video processing unit, USB 2.0 controllers, 100 Mb Ethernet interface, CAN interface and others.

All interfaces are accessible through a 315 pin MXM type III edge connector. The pin assignment is defined by emtrion's emCON standard, which ensures a pin-to-pin compatibility within all emCON CPU modules.

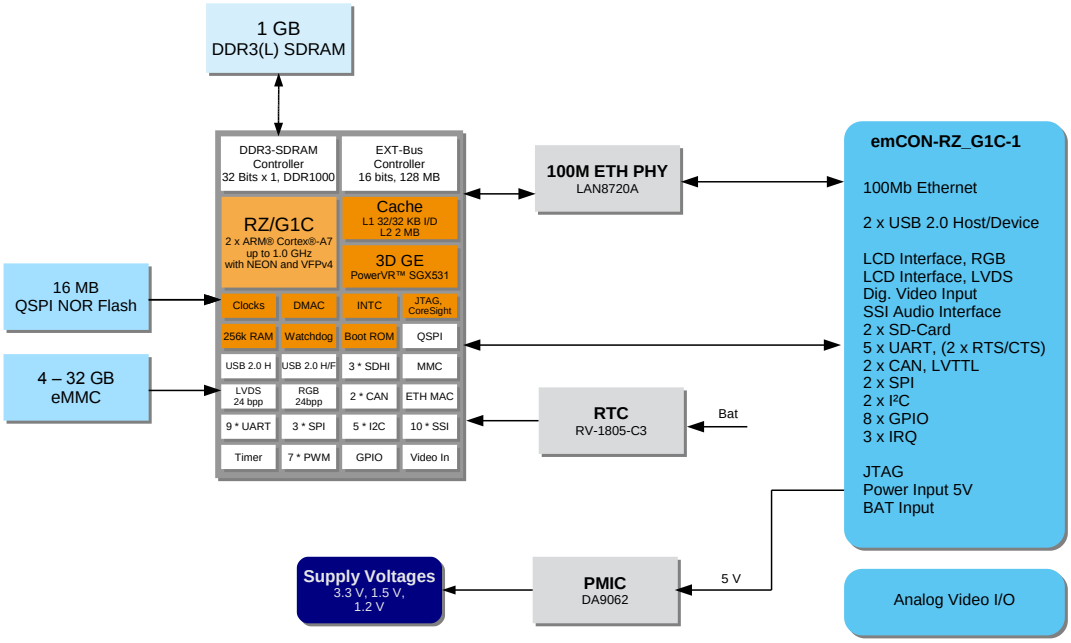
The following table lists the features and interfaces of the emCON-RZ/G1C processor module:

emCON-RZ/G1C
1 GByte DDR3L-1000 RAM
up to 32GB eMMC NAND Flash
PowerVR™ SGX531 3D graphics accelerator
1 x 10/100 Mbit Ethernet
2 x USB 2.0 Host/Device
1 x RGB interface, 18bit, max. 1080p (1920x1080)
1 x LVDS interface, 24bit max. 1080p (1920x1080)
1 x digital Video In, 8 bit
1 x analog Video In
1 x analog Video Out
1 x SSI Audio
2 x SD Card
2 x CAN (LVTTL)
5 x UART (LVTTL)
2 x SPI
2 x I2C
8 x GPIO, 3x PWM
RTC, battery backed
JTAG

The module is available in commercial temperature range 0°C to 70°C and optionally in extended temperature range -40°C to 85°C.

2 Block Diagram

The following figure shows the block diagram of the emCON-RZ/G1C.



3 Handling Precautions

Please read the following notes prior to installing the processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The module does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatically discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The emCON-RZ/G1C module is based on the processor RZ/G1C from Renesas [1]. It is equipped Dual Cortex®-A7 CPUs at 1 GHz. In addition to the CPU cores with their NEON™/VFPv4 extension and L1 and L2 Caches, the processor provides a lot of peripheral functions such as:

- DDR3-100 SDRAM controller with 32 bit data bus
- 100/1000 Mb Ethernet AVB
- 100 Mb Ethernet MAC
- Display unit with two independent channels for TFT displays with RGB and LVDS interface; resolutions up to 1080p (1920x1080) @60Hz and 24 bpp are supported
- 3D graphics engine PowerVR Series SGX531
- Two channel video input module
- Video processing unit
- Digital video Encoder and Decoder
- 2 x USB 2.0 Host with high-speed mode
- USB 2.0 Function with high-speed mode
- 3 x SD Card Host controller
- Audio interface with I2S format
- 2 x CAN controller
- 9 x UART with up to 128 byte FIFO
- 5 x I2C bus interface
- 2 x SPI interface
- JTAG debug interface

Further details of the processor can be found in the RZ/G1C Reference Manual [1].

4.1.1 Processor Clocks

The processor is clocked by a 20 MHz main clock from a quartz crystal. Three internal PLLs multiply the 20 MHz clock input to the internally needed clocks. The core clock PLL (PLL0) is set to 1.6 GHz, the peripheral PLL (PLL0) is set to 1.56 GHz.

All clocks within the processor are derived from theses PLL frequencies, via various software configurable dividers. More information about the RZ/G1C clock system is described in the CPG chapter of the RZ/G1C User's Manual [1].

4.1.2 Mode Settings

The processor mode is configured by 31 configuration pins that are sampled at the end of reset.

All of these bits are fixed and cannot be changed by the user. The boot device is set to serial flash boot at 48.75 MHz.

4.2 DDR3 SDRAM

The module incorporates two 4-Gbit DDR3(L) SDRAMs that are addressed as one 32 bits x 1 channel. The resulting RAM size is 1 GByte. The RAMs are clocked with 500 MHz (DDR3-1000 mode).

The address range of the DDR RAM is 0x40000000 – 0x7FFFFFFF.

4.3 NOR-Flash

A 16 MByte QSPI NOR Flash is connected to the QSPI interface of the RZ/G1C processor. The maximum clock rate of the interface is 97.5 MHz.

4.4 eMMC

To store the operating system and application data, normally an 8 GByte eMMC is available on the emCON-RZ/G1C module. It is connected to the MMC interface of the RZ/G1C using 8 data lines.

The signalling level of the MMC interface is sourced by VLDO2 of the PMIC DA9062. The default voltage is 3.3 V. It can be switched to 1.8 V by GPIO GP3_12 for higher data rates.

The storage capacity of the eMMC can be adapted to customer's needs by soldering different chips. Please contact emtrion GmbH for your required eMMC capacity.

4.5 SD-Card Interface

The RZ/G1C includes three SD Card Host interfaces. SDHI1 is used by the eMMC. The remaining two interfaces (SDHI0 and SDHI2) are connected to the SD Card interfaces SDC1 and SDC2 of the emCON connector.

The signaling voltage of both SD Card interfaces can be switched individually between 1.8 V and 3.3 V by the GPIOs GP5_12 for SDHI0 and GP5_19 for SDHI2. A low level selects 1.8 V and a high level selects 3.3 V.

Both interfaces can be configured to operate in Default, High Speed and SDR50 mode. Interface SDHI0 is also capable to be operated in SDR104 mode.

Watch that the active high Write Protect inputs of both interfaces are pulled high at the CPU module. The pin must be pulled low externally if a µSD socket is connected since these sockets do not incorporate a write protect switch.

4.6 Ethernet

The RZ/G1C processor incorporates two Ethernet interfaces, a 100/1000 Mbit Ethernet interface, Ethernet AVB, and a 10/100 Mbit Ethernet interface, Ethernet MAC. Only the 100 Mbit interface is available at the emCON connector, constrained by pin multiplexing.

The Ethernet MAC interface is connected to a PHY LAN8720A from Microchip by an RMII interface. The output signals of the PHY are connected to the lower data pairs of the GBE1 interface of the emCON connector. The PHY address is set to 1.

The LAN8720A is operated in REFCLK_IN mode. A 50 MHz clock from a crystal oscillator is connected to the PHY and the ETH_REFCLK input of the MAC inside the RZ/G1C.

The LED signals for speed and traffic are connected to specific pins of the GBE1 interface of the emCON connector.

4.7 USB 2.0

The RZ/G1C processor incorporates a USB 2.0 Host controller with two channels USB0and USB1. The interface USB0 is connected to the Host interface pins of the USB 2.0 OTG port of the emCON connector. The interface USB1 is connected to the USB 2.0 Host interface of the emCON connector.

The PWEN outputs of both channels are inverted to be active low at the emCON connector.

A USB Function interface is not available.

4.8 Graphic Display Interfaces

4.8.1 General

A display unit with two independently controllable channels DU0 and DU1 is incorporated in the RZ/G1C processor. The maximum resolution of the display units is 1080 x 1920 pixels which is FullHD. The display units can either display the same image or fully independent images.

Both channels can drive digital RGB24 or YC data. Additionally one of them can be connected to a LVDs interface with 4 data pairs.

4.8.2 RGB Interface

The RGB interface of the RZ/G1C processor is connected to the RGB interface of the emCON connector. Only the upper 18 colour bits of the processor are used and connected to the lower 18 bits of the emCON interface.

The signal LCD_BL_CTRL of the emCON connector is driven by the signal PWM0 of the processor. The power control signal LCD_BL_EN is driven by GP4_24. The signal LCD_PANEL_EN is driven by GP4_25.

The following table summarizes the used data and control lines.

Signal	Description
LCD_D[17:0]	18 bit colour data
LCD_PCLK	Pixel clock
LCD_HSYNC	Horizontal synchronization signal
LCD_DE	Data enable signal
LCD_VSYNC	Vertical synchronization signal
LCD_PANEL_EN	Display power enable signal, GP4_25
LCD_BL_EN	Backlight power enable signal, GP4_24
LCD_BL_CTRL	PWM signal to control the backlight, PWM0

4.8.3 LVDS Interface

The LVDS interface of the RZ/G1C processor is connected to the LVDS1 channel of the emCON connector.

The backlight control signal LVDS1_BL_CTRL is driven by the pin PWM1 of the RZ/G1C processor. The pin LVDS1_BL_EN is driven by GP1_22, the pin LVDS1_PANEL_EN is driven by GP1_1 of the processor.

The following table summarizes the signals of the LVDS interface:

Signal	Description
LVDS1_CLK_P/N	Differential LVDS clock pair
LVDS1_CH[3:0]_P/N	4 differential LVDS data pairs
LVDS1_PANEL_EN	Display power enable signal, GP1_1
LVDS1_BL_EN	Backlight power enable signal, GP1_22
LVDS1_BL_CTRL	PWM signal to control the backlight, PWM1

The colour and control signal mapping to the LVDS signal pairs can be selected from 8 different modes. Typically Mode 0 is set, which results in following mapping:

Signal	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_CH0	G2	R7	R6	R5	R4	R3	R2
LVDS_CH1	B3	B2	G7	G6	G5	G4	G3
LVDS_CH2	DE	VS	HS	B7	B6	B5	B4
LVDS_CH3	CTL	B1	B0	G1	G0	R1	R0

Further information on colour mapping can be found in [1].

The following table shows the RGB colour mapping of the pins LCD_D[23:0] at the emCON connector.

LCD_D[23:0]	RGB666 (18 bit)
LCD_D0	B2
LCD_D1	B3
LCD_D2	B4
LCD_D3	B5
LCD_D4	B6
LCD_D5	B7
LCD_D6	G2
LCD_D7	G3
LCD_D8	G4
LCD_D9	G5
LCD_D10	G6
LCD_D11	G7
LCD_D12	R2
LCD_D13	R3
LCD_D14	R4
LCD_D15	R5
LCD_D16	R6
LCD_D17	R7
LCD_D18	n/c
LCD_D19	n/c
LCD_D20	n/c
LCD_D21	n/c
LCD_D22	n/c
LCD_D23	n/c

4.9 Video Input

The emCON-RZ/G1C processor incorporates a video input module with two channels. They can be used with different digital video sources, such as video CODECs or CMOS camera modules.

The interface VIN0 of the RZ/G1C processor is connected as 8-bit parallel interface to the CPI1 interface pins of the emCON connector. The serial MIPI interface CSI2 of the emCON connector is unused.

4.10 Composite Video Encoder/Decoder

The emCON-RZ/G1C processor incorporates a video encoder with 10 bit DAC for NTSC/PAL composite output signal. It also incorporates a video decoder with ADC and sync separator for two channel NTSC/PAL composite input signal.

Since the emCON connector does not provide contacts for analogue video input and output the output signal and the input channel 1 are available at a separate 5-pin connector of type Molex PicoBlade™. The input is terminated by a 75Ω resistor. 3.3 V supply is provided to add external video circuits to the signals.

4.11 Audio Interface

The audio interfaces SSI0 and SSI4 of the RZ/G1C processor are connected to the I2S audio interface pins of the emCON connector. SSI4 is the output channel, SSI0 is the input channel. Both channels have individual word select and clock signals so that they can be operated with different data formats and clock rates.

An external audio CODEC with I2S interface can directly be connected to the interface pins.

Since the audio interface clocks are derived from the internal processor clock M2ϕ with 195 MHz they do not fit perfectly to the needed audio frequencies. For example the frequency error at 44.1 kHz sample rate is 0.13%. To get exact audio frequencies an external audio clock source can be connected to the emCON pin I2S_MCLK which is connected to the pin AUDIO_CLKA input of the RZ/G1C processor.

4.12 Serial Ports

The emCON-RZ/G1C processor incorporates a couple of serial ports with different characteristics. At the emCON connector five UART interfaces are available; two of them incorporate modem control lines.

The serial interfaces HSCIF1, HSCIF2, SCIF-3, SCIF-4 and SCIF-5 of the RZ/G1C processor are connected to the emCON connector. The following table shows the usage of the UART interfaces:

RZ/G1C peripheral	emCON interface	Modem Control
HSCIF1_A	UART_A	RTS/CTS
HSCIF2	UART_B	RTS/CTS
SCIF-3_A	UART_C	not available
SCIF-4_A	UART_D	not available
SCIF-5_C	UART_E	not available

HSCIF1 at UARTA is used as standard debug and console interface (Terminal).

4.13 I²C Interfaces

The RZ/G1C processor incorporates six I²C interfaces. Three of them are used; the interfaces I2C2, I2C3 and I2C4.

The interfaces I2C2 and I2C3 are connected to the interfaces I2C1 and I2C2 of the emCON connector. The interface I2C4 is used on board to connect the PMIC and the RTC to the processor.

The I2C components on the module have the following characteristics:

Function	Device	Interface	High Level	I²C Address (7bit)
PMIC	DA9062	I2C4	3.3 V	0x58
Real Time Clock	RV1805	I2C4	3.3 V	0x69

The interfaces at the emCON connector operate with 400 kHz clock and have 2K2 pull-up resistors to 3.3 V.

4.14 SPI Interfaces

The RZ/G1C processor incorporates three SPI interfaces MSIOFx and two QSPI interfaces. The pins of the QSPI interface QSPI1 are multiplexed with the SPI interface MSIOF0. The emCON connector provides pins for a 1-bit SPI interface and a 4-bit QSPI interface.

By default the interface QSPI of the RZ/G1C processor is connected to the interface SPI1 of the emCON connector. Alternatively the SPI interface MSIOF0 can be connected to the interface SPI1 of the emCON interface.

The following table shows the pin routing for SPI1 of the emCON interface:

RZ/G1C QSPI1	RZ/G1C MSIOF0	emCON interface
CLK	MSIOF0_SCK_A	SPI1_SCK
SSL#	MSIOF0_SS2_A#	SPI1_CS0#
IO0	MSIOF0_RXD_A	SPI1_D0
IO1	MSIOF0_TXD_A	SPI1_D1
IO2	-	SPI1_D2
IO3	MSIOF0_SS1_A#	SPI1_D3

The interface MSIOF2of the RZ/G1C processor is connected to the SPI2 interface of the emCON connector.

4.15 CAN

The RZ/G1C processor incorporates two CAN controllers, which comply with the ISO11898-1 specification. The CAN protocol specification 2.0B, with standard and extended message frames, is supported. The maximum baud rate is 1Mbps.

The TX and RX signals of both interfaces are routed to the emCON connector as LVTTL signals.

The interface CAN0_B of the processor is connected to the interface CAN1 of the emCON connector. The interface CAN1_A is connected to the interface CAN2.

CAN transceivers must be added externally.

4.16 General Purpose I/Os

The emCON interface provides eight dedicated GPIO pins which are directly connected to the RZ/G1C processor. The following table shows the signal connections:

emCON Signal	RZ/G1C Pin	Direction
GPIO_1	GP5_0	In/Out
GPIO_2	GP5_1	In/Out
GPIO_3	GP5_2	In/Out
GPIO_4	GP5_3	In/Out
GPIO_5	GP5_4	In/Out
GPIO_6	GP5_5	In/Out
GPIO_7	GP5_6	In/Out

GPIO_8	GP5_7	In/Out

All signals have LVTTL level and can drive up to +/-4 mA when configured as output.

4.17 PWM

The RZ/G1C processor incorporates seven PWM timers. Two of them are directly connected to the emCON connector:

emCON Signal	PWM Channel	Usage
LCD_BL_CTRL	PWM0	Backlight dimming
LVDS1_BL_CTRL	PWM1	Backlight dimming
PWM_FAN	-	Fan speed control

PWN_FAN is not needed. Due to the low power consumption of the processor there is no need for a fan.

The signal level of the PWM outputs is 3.3V. The output drive strength is +/-4 mA.

4.18 RTC

To enable time keeping while the module is powered off a RTC RV-1805-C3 from Micro Crystal is populated. The RTC is connected to I^2C interface I2C4 of the RZ/G1C processor. The 7-bit I^2C address of the RTC is 0x69.

The RTC is buffered by a local super capacitor, which is charged while the supply of the board is on. The charging time is about 30 min. The fully charged capacitor buffers the RTC for typically 70 days. Additionally a 3.3 V battery can be connected externally at the pin VBAT of the emCON connector. The battery current consumption of the RTC is below 60 nA.

4.19 Status LED

A bicolour LED is connected to the pins GP3_27 and GP3_28 of the RZ/G1C processor.

If only GP3_27 is high the LED is lighting red, if only GP3-28 is high the LED is lighting green. If both bits are high the LED is lighting yellow.

4.20 Interrupts

The RZ/G1C processor has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the CPU core. The interrupts can be configured to be edge triggered on rising or falling edge or to be level sensitive on high or low level.

The emCON connector specifies six interrupt inputs. Two of them are provided for touch interface controllers. Three additional inputs are generous interrupt inputs. The last interrupt input is provided as power fail input.

Four interrupts inputs are connected to the RZ/G1C processor.

The following table shows the interrupt connections of the emCON connector:

emCON Signal	RZ/G1C Pin
IRQ_TOUCH1#	**IRQ4**
IRQ_TOUCH2#	-
IRQ_1	**IRQ5**
IRQ_2	**IRQ6**
IRQ_3	-
POWERFAIL#	**NMI**

The interrupt inputs at the emCON connector are pulled high by 10 kΩ resistors.

4.21 Reset

There are several ways to cause a power reset of the board:

- 3.3V supply voltage fails
- the signal RESI# of the emCON connector is driven low
- the signal JTAG_RESI# of the emCON connector is driven low
- setting the SHUTDOWN bit in the PMIC DA9062
- clearing the bit RESOUT in register RSTOUTCR of the processor RZ/G1C
- expiration of the watchdog timer

All resets cause hardware resets of the whole board.

The duration of the reset signal is min. 100 µs. To reset external devices the reset signal is driven to pin RESO# of the emCON connector.

4.22 Power Supply

The power consumption of the module is 1.5 A at +5V, +/- 5%. The current consumption depends on the software running.

All supply voltages that are needed for the processor and the other components are generated on board by the Power Management Chip DA9062 from Dialog Semiconductor.

The output voltages of the PMICs can be configured via the I²C interface I2C4. The 7-bit I²C address of the PMIC DA9062 is 0x58.

4.22.1 Power Management Signals

POWER_ON_BASE

While the 3.3 V supply of the CPU module is switched off, it must be ensured that no external peripherals with 3.3 V interface are driving input pins. Otherwise unintended current flow might happen across the data lines.

The signal POWER_ON_BASE is used to switch off the 3.3 V supply of external components. The signal is high while the 3.3 V supply on the module is active. Otherwise the signal is low. The power switch must be realized on the carrier board.

POWERFAIL#

The signal POWERFAIL# is an input to signalize a power fail condition. The signal is connected to the NMI input of the RZ/G1C processor.

BAT

The pin BAT at the emCON connector is used as battery input for the RTC's backup power supply. The typical power consumption of the RTC at the BAT pin is < 0.5 µA.

5 emCON Interface

All interface signals of the board are available at the emCON connector.

The emCON interface is a 314 pos MXM connector. These sockets are available from various manufacturers.

The pin assignment is emtrion specific and match for the most needs of interfaces for actual embedded designs. Depending on the features of the CPUs every emtrion CPU module will use a subset of the emCON connector. More details can be found in emtrion's emCON specification.

Usage details of the connector and its electrical and mechanical characteristics can be found further down in this document.

Notes:

The pin assignment of the emCON connector is ONLY compatible with devices of emtrion's emCON-family. Insertion into a socket with another pin assignment may damage the emCON-RZ/G1C module and the carrier board.

Most of the pins are directly connected with the processor RZ/G1Cx.

6 Pin Assignments

6.1 J1, emCON Connector

Type MXM, 314 pos
Compatible carrier board connector: Aces 91782-3140M-001

Pin	Signal	Interface		Signal	Pin
1E20	GND	Power Supply		VCC_5V	2E20
1E19	GND			VCC_5V	2E19
1E18	GND			VCC_5V	2E18
1E17	GND			VCC_5V	2E17
1E16	GND			VCC_5V	2E16
1E15	GND			VCC_5V	2E15
1E14	GND			VCC_5V	2E14
1E13	GND			VCC_5V	2E13
1E12	GND			VCC_5V	2E12
1E11	GND			VCC_5V	2E11
1E10	BAT			(VCC_STANDBY)	2E10
1E9	n/c	Manufacturing	MISC	n/c	2E9
1E8	n/c			POWER_ON_BASE	2E8
1E7	n/c			IRQ4	2E7
1E6	RESET_IN#			n/c	2E6
1E5	n/c			IRQ5	2E5
1E4	JTAG_TRST#			IRQ6	2E4
1E3	JTAG_TMS			n/c	2E3
1E2	JTAG_TDO			RESO#	2E2
1E1	JTAG_TDI			RESET_IN#	40
1	JTAG_TCK			POWERFAIL#	2
3	1.8 V JTAG_VCC			(VCC_STANDBY)	4
5	JTAG_TCK			n/c	6
7	GND	POWER		n/c	8
9	HSCIF1_RXD	UART-A		n/c	10
11	HSCIF1_TXD		POWER	GND	12
13	HSCIF1_RTS		UART-C	SCIF3_RXD	14
15	HSCIF1_CTS			SCIF3_TXD	16
17	HSCIF2_RXD	UART-B	UART-D	SCIF4_RXD	18
19	HSCIF2_TXD			SCIF4_TXD	20
21	HSCIF2_RTS		UART-E	SCIF5_RXD	22
23	HSCIF2_CTS			SCIF5_TXD	24
25	GND	POWER		GND	26
27	GPIO5_0	GPIOs	PCIe	n/c	28
29	GPIO5_1			n/c	30
31	GPIO5_2			n/c	32
33	GPIO5_3			n/c	34
35	GPIO5_4			GND	36
37	GPIO5_5			n/c	38

39	GPIO5_6			n/c	**40**
41	GPIO5_7			n/c	**42**
43	GND	**POWER**		n/c	**44**
45	n/c			GND	**46**
47	n/c			n/c	**48**
49	n/c			n/c	**50**
51	n/c			n/c	**52**
53	n/c			n/c	**54**
55	n/c			GND	**56**
57	LCD_D17			n/c	**58**
59	LCD_D16			n/c	**60**
61	LCD_D15			GND	**62**
63	LCD_D14			n/c	**64**
65	LCD_D13			n/c	**66**
67	LCD_D12			n/c	**68**
69	GND			n/c	**70**
71	LCD_D11			GND	**72**
73	LCD_D10			n/c	**74**
75	LCD_D9	**RGB IF**		n/c	**76**
77	LCD_D8			n/c	**78**
79	LCD_D7			n/c	**80**
81	LCD_D6		**POWER**	GND	**82**
83	LCD_D5		**RFU**	n/c	**84**
85	LCD_D4			n/c	**86**
87	LCD_D3			n/c	**88**
89	LCD_D2			n/c	**90**
91	LCD_D1			n/c	**92**
93	LCD_D0			n/c	**94**
95	LCD_DOTCLK			n/c	**96**
97	LCD_HSYNC		**CPI2 Camera**	n/c	**98**
99	LCD_VSYNC			n/c	**100**
101	LCD_DE			n/c	**102**
103	PWM0			n/c	**104**
105	GP4_24			n/c	**106**
107	GP4_25			n/c	**108**
109	CAN1_RX	**CAN2**	**CAN1**	CAN0_RX	**110**
111	CAN1_TX			CAN0_TX	**112**
113	GND	**POWER**	**POWER**	GND	**114**
115	QSPI1_SCK			MSIOF2_SS2#	**116**
117	QSPI1_SSL#			MSIOF2_SS1#	**118**
119	QSPI1_IO0	**SPI 1**	**SPI 2**	MSIOF2_TXD	**120**
121	QSPI1_IO1			MSIOF2_RXD	**122**
123	QSPI1_IO2			MSIOF2_SCK	**124**
125	QSPI1_IO3				
The pins 126 - 132 are used for mechanical coding and not available as electrical pins					
133	VIN0_D0	**VIN3 Camera**	**MIPI_CSI2**	n/c	**134**

135	VIN0_D1		**Camera**	n/c	**136**
137	VIN0_D2			n/c	**138**
139	VIN0_D3			n/c	**140**
141	VIN0_D4			n/c	**142**
143	VIN0_D5			n/c	**144**
145	VIN0_D6			n/c	**146**
147	VIN0_D7			n/c	**148**
149	VIN0_CLK			n/c	**150**
151	VIN0_HSYNC			n/c	**152**
153	VIN0_VSYNC		**POWER**	GND	**154**
155	GND	**POWER**	**I2C1**	SCL2	**156**
157	PWM1	**LVDS1 Control**		SDA2	**158**
159	GP1_22		**I2C2**	SCL3	**160**
161	GP1_1			SDA3	**162**
163	GND	**POWER**	**LVDS2**	n/c	**164**
165	LVDS_D0_P	**LVDS1**		n/c	**166**
167	LVDS_D0_N			n/c	**168**
169	LVDS_D1_P			n/c	**170**
171	LVDS_D1_N			n/c	**172**
173	LVDS_D2_P			n/c	**174**
175	LVDS_D2_N			n/c	**176**
177	LVDS_D3_P			n/c	**178**
179	LVDS_D3_N			n/c	**180**
181	LVDS_CLK_P			n/c	**182**
183	LVDS_CLK_N		**POWER**	GND	**184**
185	GND	**POWER**	**HDMI**	n/c	**186**
187	n/c	**SPDIF**		n/c	**188**
189	n/c			n/c	**190**
191	SSI_D0	**I2S Audio**		n/c	**192**
193	SSI_D4			n/c	**194**
195	SSI_WS4			n/c	**196**
197	SSI_SCK4			n/c	**198**
199	SSI_WS0129			n/c	**200**
201	SSI_SCK0129		**POWER**	GND	**202**
203	ACLK		**HDMI Control**	n/c	**204**
205	n/c	**SATA**		n/c	**206**
207	n/c			n/c	**208**
209	n/c			n/c	**210**
211	n/c		**POWER**	GND	**212**
213	GND	**POWER**		GND	**214**
215	n/c	**USB OTG**	**USB Host**	USB1_DP	**216**
217	USB0_DP			USB1_DN	**218**
219	USB0_DN			USB1_VBUS	**220**
221	USB0_VBUS			USB1_OC#	**222**
223	USB0_OC#			USB2_PEN#	**224**
225	USB0_PEN#		**USB3.0**	n/c	**226**

227	n/c			n/c	**228**
229	n/c		**POWER**	GND	**230**
231	GND	**POWER**	**USB3.0**	n/c	**232**
233	n/c			n/c	**234**
235	n/c		**POWER**	GND	**236**
237	GND	**POWER**		SD2_CLK	**238**
239	SD0_CLK			SD2_CMD	**240**
241	SD0_CMD			SD2_D0	**242**
243	SD0_D0		**SD Card 2**	SD2_D1	**244**
245	SD0_D1			SD2_D2	**246**
247	SD0_D2			SD2_D3	**248**
249	SD0_D3			SD2_CD#	**250**
251	SD0_CD#			SD2_WP	**252**
253	SD0_WP		**POWER**	GND	**254**
255	GND	**POWER**		n/c	**256**
257	ETH_TXP			n/c	**258**
259	ETH_TXN			n/c	**260**
261	ETH_RXP		**Ethernet2**	n/c	**262**
263	ETH_RXN			n/c	**264**
265	n/c	**Ethernet1**		n/c	**266**
267	n/c			n/c	**268**
269	n/c			n/c	**270**
271	n/c		**POWER**	GND	**272**
273	GND	**POWER**		n/c	**274**
275	ETH_LED_100M#			n/c	**276**
277	n/c		**Ethernet2**	n/c	**278**
279	ETH_LED_TRAFFIC#	**Ethernet1**		n/c	**280**
281	n/c				

7 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	digital input
O	digital output
I/O	digital bidirectional
O(OD)	digital open drain output

PU xK	x KΩ pullup resistor
PD xK	x KΩ pulldown resistor
SR xR	x Ω series resistor
IPU xK	processor internal x KΩ pullup resistor
IPD xK	transistor internal x KΩ pulldown resistor

7.1 J1, emCON Connector

Name	RZ/G1C Pin	GPIO	Direction	Termination	Volt	Max. Current	Description
Ethernet 1							
ETH_TXP	-	-	A I/O	-	-	N/A	ETH diff. transmit pair
ETH_TXN	-	-	A I/O	-	-	N/A	
ETH_RXP	-	-	A I/O	-	-	N/A	ETH diff. receive pair
ETH_RXN	-	-	A I/O	-	-	N/A	
ETH_LED_100#	-	-	O	-	3.3V	20mA	10/100# Speed indication
ETH_LED_TRAFFIC#	-	-	O	-	3.3V	20mA	Traffic indication

USB Host							
USBH_PEN#	#AD30	GP5_22	O		3.3V	32mA	USB power enable
USBH_OC#	AC30	GP5_23	I	-	3.3V	N/A	USB overcurrent signal from power switch
USBH_DP	AK31	-	I/O	-	-	N/A	USB 2.0 diff. data pair
USBH_DM	AJ31	-	I/O	-	-	N/A	

USB OTG							
USBOTG_ID	AC29	GP5_20	I	PU 10K	3.3V	N/A	USB ID signal for OTG functionality
USBOTG_PEN#	AC28	GP5_18	O	-	3.3V	16mA	Host: USB power
USBOTG_OC#	AD28	GP5_19	I	PU 10K	3.3V	N/A	Host: USB overcurrent
USBOTG_VBUS	AD28	GP5_19	I	PD 32K	4.2V – 5.5V	N/A	Device: VBUS
USBOTG_DP	AF31	-	I/O	-	-	N/A	USB 2.0 diff. data pair
USBOTG_DM	AE31	-	I/O	-	-	N/A	

UART							
UART-A_TXD	AH5	GP0_21	O	PU 10K	3.3V	8mA	UART transmit data
UART-A_RXD	AL5	GP0_24	I	-	3.3V	N/A	UART receive data
UART-A_RTS	AJ5	GP0_22	O	-	3.3V	8mA	UART modem control
UART-A_CTS	AJ4	GP0_25	I	-	3.3V	N/A	UART modem control
UART-B_TXD	T28	GP4_23	O	PU 10K	3.3V	8mA	UART transmit data
UART-B_RXD	T26	GP4_22	I	-	3.3V	N/A	UART receive data
UART-B_RTS	V31	GP4_25	O	-	3.3V	8mA	UART modem control
UART-B_CTS	R25	GP4_24	I	-	3.3V	N/A	UART modem control
UART-C_TXD	AE5	GP1_18	O	-	3.3V	4mA	UART transmit data
UART-C_RXD	AC1	GP1_12	I	-	3.3V	N/A	UART receive data
UART-D_TXD	AK11	GP5_30	O	PU 10K	3.3V	4mA	UART transmit data
UART-D_RXD	AJ11	GP5_31	I	-	3.3V	N/A	UART receive data

UART-E_TXD	AH1	GP1_21	O	-	3.3V	4mA	UART transmit data
UART-E_RXD	AD2	GP1_20	I	-	3.3V	N/A	UART receive data
CAN							
CAN1_TX	P30	GP4_4	O	-	3.3V	8mA	CAN transmit data
CAN1_RX	P29	GP4_5	I	PU 10K	3.3V	N/A	CAN receive data
CAN2_TX	P27	GP4_6	O	-	3.3V	8mA	CAN transmit data
CAN2_RX	R26	GP4_7	I	PU 10K	3.3V	N/A	CAN receive data
LCD (RGB Display)							
LCD_PIXCLK	Y25	GP5_2	O	-	3.3V	8mA	LCD dot clock
LCD_DISP	W26	GP5_16	O	-	3.3V	8mA	LCD data enable signal
LCD_VSYNC	U30	GP4_15	O	-	3.3V	8mA	LCD frame sync
LCD_HSYNC	U31	GP4_14	O	-	3.3V	8mA	LCD line sync
LCD_D0	V26	GP5_8	O	-	3.3V	8mA	LCD B2
LCD_D1	V27	GP5_9	O	-	3.3V	8mA	LCD B3
LCD_D2	U26	GP5_10	O	-	3.3V	8mA	LCD B4
LCD_D3	U25	GP5_11	O	-	3.3V	8mA	LCD B5
LCD_D4	Y31	GP5_12	O	-	3.3V	8mA	LCD B6
LCD_D5	V25	GP5_13	O	-	3.3V	8mA	LCD B7
LCD_D6	AA30	GP4_27	O	-	3.3V	8mA	LCD G2
LCD_D7	W25	GP4_30	O	-	3.3V	8mA	LCD G3
LCD_D8	V28	GP5_7	O	-	3.3V	8mA	LCD G4
LCD_D9	W28	GP5_14	O	-	3.3V	8mA	LCD G5
LCD_D10	W29	GP5_15	O	-	3.3V	8mA	LCD G6
LCD_D11	AB28	GP5_4	O	-	3.3V	8mA	LCD G7
LCD_D12	P26	GP4_16	O	-	3.3V	8mA	LCD R2
LCD_D13	U29	GP4_17	O	-	3.3V	8mA	LCD R3
LCD_D14	U27	GP4_18	O	-	3.3V	8mA	LCD R4

LCD_D15	T25	GP4_19	O	-	3.3V	8mA	LCD R5
LCD_D16	V29	GP4_20	O	-	3.3V	8mA	LCD R6
LCD_D17	U28	GP4_21	O	-	3.3V	8mA	LCD R7
LCD_PANEL_EN	Y30	GP4_29	O	-	3.3V	8mA	LCD panel power enable
LCD_BL_EN	AA29	GP4_28	O	-	3.3V	8mA	LCD backlight power enable
LCD_BL_CTRL	AG6	PWM4	O	-	3.3V	8mA	LCD backlight brightness control
LVDS 1							
LVDS_CLK_P	AG17	-	O	-	1,8V	N/A	LVDS diff clock pair
LVDS_CLK_N	AG18	-	O	-	1,8V	N/A	
LVDS_TX0_P	AJ18	-	O	-	1,8V	N/A	LVDS diff data pair
LVDS_TX0_N	AJ19	-	O	-	1,8V	N/A	
LVDS_TX1_P	AG19	-	O	-	1,8V	N/A	LVDS diff data pair
LVDS_TX1_N	AG20	-	O	-	1,8V	N/A	
LVDS_TX2_P	AL18	-	O	-	1,8V	N/A	LVDS diff data pair
LVDS_TX2_N	AL17	-	O	-	1,8V	N/A	
LVDS_TX3_P	AJ17	-	O	-	1,8V	N/A	LVDS diff data pair
LVDS_TX3_N	AJ16	-	O	-	1,8V	N/A	
LVDS_PANEL_EN	-	-	O	PD 2K2	3.3V	4mA	LVDS panel power enable
LVDS_BL_EN	-	-	O	PD 2K2	3.3V	4mA	LVDS backlight power enable
LVDS_BL_CTRL	AH6	PWM5	O	-	3.3V	8mA	LVDS backlight brightness control
CPI1 (Camera Input)							
VIN0_D0	AF9	GP0_0	I	-	3.3V	8mA	Video image input data
VIN0_D1	AG9	GP0_1	I	-	3.3V	8mA	Video image input data
VIN0_D2	AH9	GP0_2	I	-	3.3V	8mA	Video image input data
VIN0_D3	AJ9	GP0_3	I	-	3.3V	8mA	Video image input data
VIN0_D4	AK9	GP0_4	I	-	3.3V	8mA	Video image input data
VIN0_D5	AL9	GP0_5	I	-	3.3V	8mA	Video image input data

VIN0_D6	AF8	GP0_6	I	-	3.3V	8mA	Video image input data
VIN0_D7	AG8	GP0_7	I	-	3.3V	8mA	Video image input data
VIN0_PIXCLK	AK1	GP1_23	I	-	3.3V	8mA	Video clock
VIN0_HSYNC	AE3	GP1_16	I	-	3.3V	8mA	Video line sync
VIN0_VSYNC	AE4	GP1_17	I	-	3.3V	4mA	Video frame sync
SD Card Interface 1							
SDC1_D0	W2	GP3_2	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_D1	V7	GP3_3	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_D2	V6	GP3_4	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_D3	V5	GP3_5	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_CMD	V4	GP3_1	I/O	PU 47K	1.8V/3.3V	16mA	CMD signal
SDC1_CLK	V1	GP3_0	O	SR 22R	1.8V/3.3V	16mA	SDC clock
SDC1_CD#	W3	GP3_6	I	PU 10K	3.3V	N/A	Card detect
SDC1_WP	W4	GP3_7	I	PD 10K	3.3V	N/A	Write protect
SD Card Interface 2							
SDC2_D0	R5	GP3_18	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_D1	R4	GP3_19	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_D2	R3	GP3_20	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_D3	T5	GP3_21	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_CMD	T4	GP3_17	I/O	PU 47K	1.8V/3.3V	16mA	CMD signal
SDC2_CLK	R1	GP3_16	O	SR 22R	1.8V/3.3V	16mA	SDC clock
SDC2_CD#	T2	GP3_22	I	PU 10K	3.3V	N/A	Card detect
SDC2_WP	T3	GP3_23	I	PD 10K	3.3V	N/A	Write protect
SPI1							
SPI1_SS0#	R27	GP4_10	O		3.3V	8mA	SPI slave select
SPI1_SS1#	T31	GP4_11	O		3.3V	8mA	SPI slave select
SPI1_SCK	R31	GP4_8	O		3.3V	8mA	SPI clock
SPI1_MISO	R29	GP4_13	I		3.3V	8mA	SPI data from slave

SPI1_MOSI	T29	GP4_12	O		3.3V	8mA	SPI data to slave
SPI2							
SPI2_SS0#	AL2	GP0_30	O		3.3V	8mA	SPI slave select
SPI2_SS1#	AH3	GP0_31	O		3.3V	8mA	SPI slave select
SPI2_SCK	AL4	GP0_27	O		3.3V	8mA	SPI clock
SPI2_MISO	AL3	GP0_29	I		3.3V	8mA	SPI data from slave
SPI2_MOSI	AK3	GP0_28	O		3.3V	8mA	SPI data to slave
I2C1							
I2C1_SCL	AG15	-	I/O	PU 2K2	3.3V	15mA	I^2C clock
I2C1_SDA	AF15	-	I/O (OD)	PU 2K2	3.3V	15mA	I^2C data
I2C2							
I2C2_SCL	AC27	GP5_5	I/O	PU 2K2	3.3V	8mA	I^2C clock
I2C2_SDA	AB27	GP5_6	I/O (OD)	PU 2K2	3.3V	8mA	I^2C data
Audio SSI							
AUDIO_RXD	AD4	GP1_27	I		3.3V	N/A	Audio input data
AUDIO_TXD	AD5	GP1_26	O		3.3V	4mA	Audio output data
AUDIO_TXC	AC5	GP1_24	I/O		3.3V	4mA	Audio transmit bit clock
AUDIO_TXFS	AC6	GP1_25	I/O		3.3V	4mA	Audio transmit frame select
AUDIO_RXC	AC5	GP1_24	I/O		3.3V	4mA	Audio receive bit clock
AUDIO_RXFS	AC6	GP1_25	I/O		3.3V	4mA	Audio receive frame select
ACLK	W31	GP4_26	I		3.3V	N/A	Audio master clock
General Purpose I/O							
GPIO1	AG1	GP1_0	I/O		3.3V	8mA	digital input / output
GPIO2	AG2	GP1_1	I/O		3.3V	8mA	digital input / output
GPIO3	AG3	GP1_2	I/O		3.3V	8mA	digital input / output
GPIO4	AG4	GP1_3	I/O		3.3V	8mA	digital input / output

GPIO5	AD1	GP1_10	I/O		3.3V	8mA	digital input / output
GPIO6	AJ2	GP1_11	I/O		3.3V	8mA	digital input / output
GPIO7	AC2	GP1_13	I/O		3.3V	8mA	digital input / output
GPIO8	AC3	GP1_14	I/O		3.3V	8mA	digital output only
Manufacturing							
JTAG_TCK	AE14		I	PU 10K	1.8V	N/A	JTAG clock (JTAG_TCK and JTAG_RTCK are shorted)
JTAG_TMS	AF14		I	PU 10K	1.8V	N/A	JTAG mode select
JTAG_TRST#	AG16		I	PD 1K	1.8V	N/A	JTAG test reset
JTAG_TDI	AH14		I	PU 10K	1.8V	N/A	JTAG data input
JTAG_TDO	AH12		O		1.8V	1mA	JTAG data output
JTAG_RTCK	AE18		O	PU 10K	1.8V	N/A	JTAG return clock (JTAG_TCK and JTAG_RTCK are shorted)
JTAG_MOD	-	-	-	-	-	-	Mode selection JTAG/Boundary Scan
JTAG_RESET#	-	-	-	-	1.8V	N/A	JTAG reset
JTAG_VCC					1.8V		JTAG voltage reference
Miscellaneous							
IRQ_1	AJ13	GP5_26	I	PU 10K	3.3V	N/A	Interrupt input
IRQ_2	AH13	GP5_27	I	PU 10K	3.3V	N/A	Interrupt input
IRQ_3	-	-	-	-	-	-	Interrupt input
IRQ_TOUCH1#	AA25	GP5_24	I	PU 10K	3.3V	N/A	Interrupt input for touch controller
POWERFAIL#	AG12	NMI	I	PD 20K	5V	N/A	Power Fail interrupt
PWM_FAN	AL7	PWM3	O		3.3V	8mA	PWM signal for fan control
RESI#			I	PU 10K	3.3V	N/A	Reset input from carrier board
RESO#			O		3.3V	20mA	Reset output to carrier board
POWER_ON_BASE			O		3.3V	20mA	Power enable signal for the 3.3V baseboard supply

SUSPEND#	O		3.3V	20mA	Power switching signal for VCC_5V
ON_OFF#	I	PU 100K	5V	N/A	Power management signal
Power Supply					
BAT	-	-	2.0V – 3.3V	N/A	Battery backup supply for RTC
VCC_5V	-	-	-	N/A	+ 5V supply
GND	-	-	-	N/A	Ground

8 Technical Characteristics

8.1 Electrical Specifications

Supply voltage	5V, +/-5%
Current consumption	up to 1.5 A

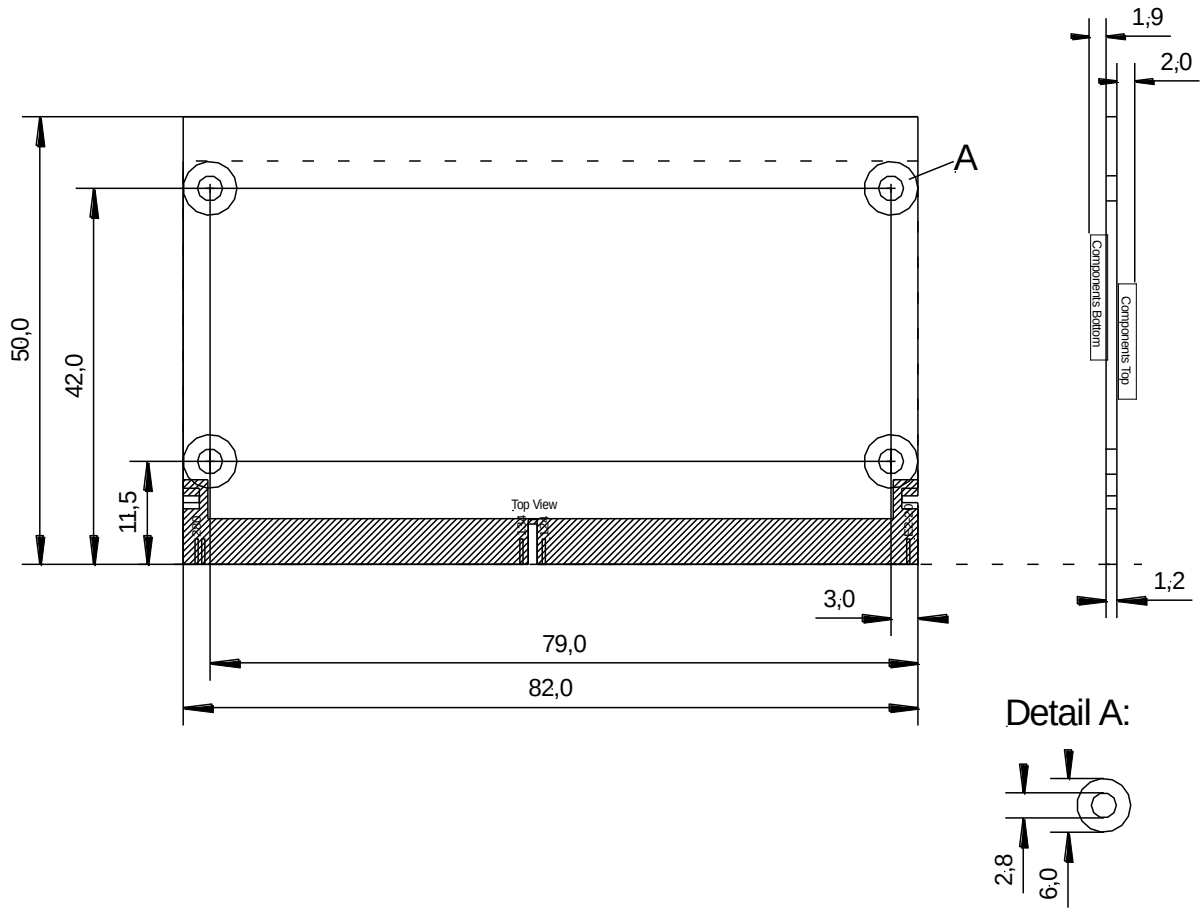
8.2 Environmental Specifications

Operating temperature Standard: Extended: **Storage temperature**	 0 ... +70°C -40 ... +85°C -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

8.3 Mechanical Specifications

Weight	approx. 19 g
Board	Glasepoxi FR-4, UL-listed, 10 layers
Dimensions	82.2 mm x 50.0 mm x 5.0 mm

9 Dimensional Drawing



10 References

[1] RZ/G1C
User's Manual: Hardware
R01UH0695EJ0040, Rev.0.40, Oct. 31, 2016