emCON-RZ/G1M - Hardware Manual

Hardware Manual

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emtrion GmbH

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Rev	Date/Signature	Changes
1	28.11.16/Bue	First release
2	20.03.17/Bue	Type of 3D Graphics controller corrected in chapter 3.1, clock characteristics corrected in chapter 3.1.1
3	15.05.17/Bue	Typos corrected in chapter 6.1
4	23.04.18/Bue	Solder bridge BR1 added in chapter 3.7 and in block diagram in chapter 1

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Introduction

The emCON-RZ/G1M module is a CPU board of emtrion's emCON-family based on the RZ/G1M processor from Renesas.

The RZ/G1M processor is a multi chip module which incorporates two Cortex™-A15 MPCore™ cores. The cores run up to 1.5 GHz and are accompanied by a variety of functions required for rich graphics and industrial applications. These functions include a 3D graphics accelerator, video processing unit, USB3.0 and USB 2.0 controllers, PCIe interface, SATA interface, Gb Ethernet interface, CAN interface and others.

All interfaces are accessible through a 315 pin MXM type III edge connector. The pin assignment is defined by emtrion's emCON standard, which ensures a pin-to-pin compatibility within all emCON CPU modules.

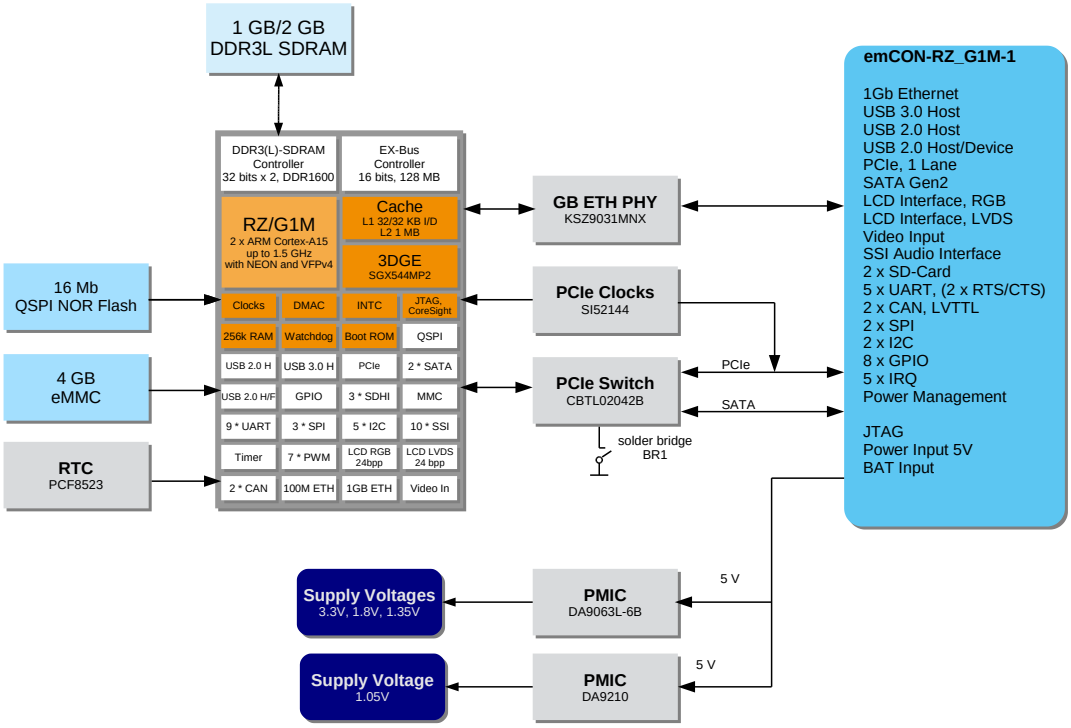
The following table lists the features and interfaces of the emCON-RZ/G1M processor module:

emCON-RZ/G1M
1 GByte DDR3L-1600 RAM
up to 32GB eMMC NAND Flash
3D graphics engine PowerVR™SGX544MP2
1 x 100/1000 Mbit Ethernet
1 x USB 3.0 Host
1 x USB 2.0 Host
1 x USB 2.0 Device
1 x PCIe (1 lane)
1 x LCD Interface 18bit max. 1080p (1920x1080)
1 x LVDS 24bit max. 1080p (1920x1080)
1 x Video In, 8 bit
1 x SSI Audio
1 x SATA II
2 x SD Card
2 x CAN (LVTTL)
5 x UART (LVTTL)
2 x SPI
2 x I2C
8 x GPIO, 3x PWM
RTC, battery backed
JTAG

The module is available in commercial temperature range 0°C to 70°C and in extended temperature range -40°C to 85°C.

1 Block Diagram

The following figure shows the block diagram of the emCON-RZ/G1M.



2 Handling Precautions

Please read the following notes prior to installing the processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The module does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatically discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

3 Functional Description

3.1 Processor

The emCON-RZ/G1M module is based on the processor RZ/G1M from Renesas [1]. It incorporates two Cortex™-A15 cores which run at up to 1.5 GHz. In addition to the CPU cores with their NEON™/VFPv4 extension and L1 and L2 Caches, the processor provides a lot of peripheral functions such as:

- DDR3L-1600 SDRAM controller
- 100/1000 Mb Ethernet MAC
- Two SERDES interfaces which can be configured as either
    - SATA II interface
    - USB 3.0 Host
    - PCIe interface
- Two Image Processing Units which includes
    - 2 x independent display unit for TFT displays with RGB and LVDS interface; resolutions up to 1080p (1920x1080) @60Hz and 24 bpp are supported
    - 3D graphics engine PowerVR™SGX544MP2
    - 2D graphics rendering function
    - 3 channel video input module
    - Video processing unit
- USB 2.0 Host with high-speed mode
- USB 2.0 Function with high-speed mode
- 4 x SD Card Host controller
- Audio interface with I2S format
- 2 x CAN controller
- 9 x UART with up to 128 byte FIFO
- 4 x I2C bus interface
- 2 x SPI interface
- Watchdog timer
- JTAG debug interface

Further details of the processor can be found in the RZ/G1M Reference Manual [1].

3.1.1 Processor Clocks

The processor is clocked by a 20 MHz main clock from a quartz crystal. Three internal PLLs multiply the 20 MHz clock input to the internally needed clocks. The core clock PLL (PLL1) is set to 3.12 GHz, the peripheral PLL (PLL0) is set to 2.6 GHz.

All clocks within the processor are derived from theses PLL frequencies, via various software configurable dividers. More information about the RZ/G1M clock system is described in the CPG chapter of the Common RZ/G Series User Manual [1].

3.1.2 Mode Settings

The processor mode is configured by 25 configuration pins that are sampled at the end of reset.

All bits are fixed besides MD24 which is used to configure the PCIEC1 interface as either SATA or PCIe function. Setting is done by solder bridge BR1. Watch that changing this configuration bit demands to change the software accordingly.

3.2 DDR3 SDRAM

The module incorporates up to 2 GByte DDR3L SDRAM which are addressed as either 32 bits x 1 channel or 32 bits x 2 channels. The RAMs are clocked with 800 MHz (DDR3-1600 mode).

RAM size	Start address	End address
1GB	0x00 4000 0000	0x00 7FFF FFFF
2GB	0x00 4000 0000	0x00 BFFF FFFF

Please contact emtrion GmbH for your required RAM size.

3.3 NOR-Flash

A 16 MByte QSPI NOR Flash is connected to the QSPI interface of the RZ/G1M processor. This is the standard boot device and cannot be changed.

The clock rate of the interface is limited to 48.75 MHz by the processor.

3.4 eMMC

To store the operating system and application data, normally an 8 GByte eMMC is available on the emCON-RZ/G1M module. It is connected to the MMC interface of the RZ/G1M using 8 data lines.

The capacity of the eMMC can be between selected between 4 GB and 32 GB depending on the ordering code.

Please contact emtrion GmbH for your required eMMC capacity.

3.5 SD-Card Interface

The RZ/G1M includes three SD Card Host interfaces. Two of them (SDHI0 and SDHI2) are connected to the SD Card interfaces SDC1 and SDC2 of the emCON connector.

The signaling voltage of both SD Card interfaces can be switched individually between 1.8 V and 3.3 V by the GPIOs GP2_15 and GP2_16. A low level selects 1.8 V and a high level selects 3.3 V.

Both interfaces can be configured to operate in Default, High Speed and SDR50 mode. Interface SDHI0 is also capable to be operated in SDR104 mode.

Watch that the active high Write Protect inputs of both interfaces are pulled high at the CPU module. The pin must be pulled low externally if a µSD socket is connected since these sockets do not incorporate a write protect switch.

3.6 Ethernet

The RZ/G1M processor incorporates a GBit Ethernet interface, called Ethernet AVB, and a 100 Mbit Ethernet interface, called Ethernet MAC. Both Ethernet interfaces share the same pins. Therefore only the Ethernet AVB interface is available.

An Ethernet PHY KSZ9031MNX from Micrel is used to connect the Ethernet AVB interface to the GBit Ethernet interface 1 of the emCON connector. The PHY address is set to 1.

The LED signals for speed and traffic are connected to the appropriate pins.

An appropriate 1:1 transformer with a 100nF capacitor to GND at each center tap pin must be added externally. The center tap pin shall not be supplied with 3.3V!

The emCON pin GBE1_LED_10_100# and GBE1_LED_1000# are both connected to the LED1 pin of the Ethernet PHY and light if a link is established. Therefore the link speed has to be determined by software.

The emCON pin GBE1_LED_TRAFFIC# is connected to the LED2 pin of the Ethernet PHY and indicates if data is transferred (“blinking light” = traffic).

3.7 SATA, PCIe, USB3.0

The RZ/G1M processor incorporates two PCIe physical interfaces that can be configured to work as SATA, PCIe or USB3.0 interface. Interface 0 can be configured as SATA0 or USB3.0. Interface 1 can be configured as SATA1or PCIe. The configuration is done by mode pins after reset.

At the emCON-RZ/G1M module the interface PCIEC0 is configured to operate as USB3.0 interface. The signals are routed to the USB3.0 super speed pins of the USB Host interface of the emCON connector.

The configuration of interface PCIEC1 is selectable to be configured as PCIe interface or as SATA1 interface. These signals are routed to the emCON connector by a PCIe multiplexer/demultiplexer CBTL02042A from NXP to either the SATA or the PCIe lane 1 interface.

The configuration is controlled by solder bridge BR1.

State of BR1	Configuration
open	PCIe
closed	SATA

The signal PCIE_DISABLE# is not driven. The signal PCIE_RST# is driven by the GPIO GP7_7.

The PCIe clock lines are driven by a one channel of a quad channel clock synthesizer SI52144 from Silicon Labs. Two other channels drive the PCIe interfaces of the RZ/G1M processor. The clock generator can be accessed by the I^2C interface I2C4 at address 0x6B if needed.

No AC coupling capacitors are fit in the signal paths of the PCIe interface. They must be populated externally on a connected module. The transmit signal pair of the USB3.0 interface and both signal pairs of the SATA interface have capacitors populated.

3.8 USB 2.0

The RZ/G1M processor incorporates a USB 2.0 Host interface USB1 and a USB 2.0 Host/Function interface USB0. Both USB 2.0 interfaces are connected to the emCON.

USB1 is connected to the USB 2.0 pins of the USB Host interface- The pin GP7_23 of the RZ/G1M processor is used as active high USB Host Power Enable output. The signal is inverted and connected to the active low signal USBH_PEN# of the emCON interface. The pin GP6_30 is the corresponding overcurrent input of the USB Host interface.

USB0 is connected to the USB OTG interface of the emCON connector. The interface USB0 is not a real USB OTG interface but can be configured to be either Host or Function. The Host/Function selection is done by the signal USBOTG_ID. When USBOTG_ID is low the Host interface is selected otherwise the Function interface. The signal is pulled high by a 10K resistor and connected to pin GP2_25 of the RZ/G1M processor.

If the USB0 interface is configured as Host interface the pin GP7_25 of the RZ/G1M processor is used as USB OTG Power Enable output. The signal is inverted and connected to the active low signal USBOTG_PEN# of the emCON interface. The pin GP7_24 is the corresponding overcurrent input.

If the USB0 interface is configured as Function interface the pin GP7_24 becomes the VBUS detection input. The selection is controlled automatically by the USBOTG ID input pin.

3.9 Graphic Displays

Two display unit interfaces DU0 and DU1 are available at the RZ/G1M processor. The DU0 interface is an LVDS interface with 24 bpp color depth. The DU1 interface is a standard 24 bpp RGB interface with LVTTL signals. Both display units can display the same image on both monitors or fully independent images.

The maximum resolution of both display units is 1080 x 1920 pixels which is FullHD. A frame rate of 60 fps at that resolution would demand a 148.5 MHz pixel clock. Since the clock is derived from the internal processor clock ZXϕ with 520MHz only 130 MHz can be selected.

3.9.1 LVDS Interface

DU0 is connected to the LVDS1 interface of emCON connector. The backlight control signal LVDS1_BL_CTRL is driven by the pin PWM2 of the RZ/G1M processor. The pin LVDS1_BL_EN is driven by GP0_6 and the pin LVDS1_PANEL_EN is driven by GP0_5.

The following table describes the signals of LVDS1 interface:

Signal	Description
LVDS1_CLK_P/N	Differential LVDS clock pair
LVDS1_CH[3:0]_P/N	Differential LVDS data signal pairs
LVDS1_PANEL_EN	Display power enable signal, GP0_5
LVDS1_BL_EN	Backlight power enable signal, GP0_6
LVDS1_BL_CTRL	PWM signal to control the backlight, PWM2

The colour and control signal mapping to the LVDS signal pairs can be selected from 8 different modes. Typically Mode 0 is set, which results in following mapping:

Signal	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_CH0	G2	R7	R6	R5	R4	R3	R2
LVDS_CH1	B3	B2	G7	G6	G5	G4	G3
LVDS_CH2	DE	VS	HS	B7	B6	B5	B4
LVDS_CH3	CTL	B1	B0	G1	G0	R1	R0

Further information on colour mapping can be found in [1].

3.9.2 RGB Interface

DU1 is connected to the RGB interface of emCON. Only the upper 18 colour bits and a set of control lines are available at the emCON connector. The backlight control signal LCD_BL_CTRL is driven by the pin PWM1 of the RZ/G1M processor. The pin LCD_BL_EN is driven by GP0_13 and the pin LCD_PANEL_EN is driven by GP0_12.

The following table describes the function of the data and control lines.

Signal	Description
LCD_D[17:0]	18 bit color data
LCD_VSYNC	Vertical synchronization signal
LCD_HSYNC	horizontal synchronization signal
LCD_DE	Data enable signal, if active colour data are valid
LCD_PCLK	Display clock
LCD_PANEL_EN	Display power enable signal, GP0_12
LCD_BL_EN	Backlight power enable signal, GP0_13
LCD_BL_CTRL	PWM signal to control the backlight, PWM1

The following table shows the RGB colour mapping of the pins LCD_D[23:0] at the emCON connector.

LCD_D[23:0]	RGB666 (18bit)
LCD_D0	B2
LCD_D1	B3
LCD_D2	B4
LCD_D3	B5
LCD_D4	B6
LCD_D5	B7
LCD_D6	G2
LCD_D7	G3
LCD_D8	G4
LCD_D9	G5
LCD_D10	G6
LCD_D11	G7
LCD_D12	R2
LCD_D13	R3
LCD_D14	R4
LCD_D15	R5
LCD_D16	R6
LCD_D17	R7
LCD_D18	n/c
LCD_D19	n/c
LCD_D20	n/c
LCD_D21	n/c
LCD_D22	n/c
LCD_D23	n/c

3.10 Video Input

The emCON-RZ/G1M processor incorporates three video input units which can be used with different video sources, such as video CODECs or CMOS camera modules.

Only the interface VIN0 of the RZ/G1M processor is available at the CPI1 interface pins of the emCON connector. The serial MIPI interface CSI2 of the emCON connector is unused.

3.11 Audio Interface

The audio interfaces SSI3 and SSI4 of the RZ/G1M processor are connected to the I2S audio interface pins of the emCON connector. SSI3 is the output channel, SSI4 is the input channel. Both channels can be operated independently with different data format and clock rates.

An external audio CODEC with I2S interface can directly be connected to the interface pins.

Since the audio interface clocks are derived from the internal processor clock M2ϕ with 195 MHz they do not fit perfectly to the needed audio frequencies. For example the frequency error at 44.1 kHz sample rate is 0.13%. To get exact audio frequencies an external audio clock source can be

connected to the emCON pin I2S_MCLK which is connected to the pin AUDIO_CLKA of the RZ/G1M processor.

3.12 Serial Ports

The emCON-RZ/G1M processor has six serial ports with 64 byte FIFO, SCIF, and additionally three high speed serial ports HSCIF with 128 byte FIFO. All ports have modem control lines RTS and CTS.

At the emCON connector 5 UART interfaces are specified, two of them incorporate modem control lines.

The following table shows the usage of the UART interfaces:

RZ/G1M peripheral	emCON interface	Modem Control
HSCIF0	UART_A	RTS/CTS
HSCIF1	UART_B	RTS/CTS
SCIF2	UART_C	not available
SCIF3	UART_D	not available
SCIF4	UART_E	not available

UARTA is used as standard debug and communication interface (Terminal).

3.13 I²C Interfaces

The RZ/G1M processor incorporates six I²C interfaces.

The interfaces I2C0 and I2C1 of the processor RZ/G1M are connected to the interfaces I2C1 and I2C2 of the emCON connector. The interface I2C4 is used on board to connect the RTC and the PCI clock generator to the processor. The interface I2C5 is used on board to connect the PMICs to the processor.

The internally used I2C components on the module have the following characteristics:

Function	Device	Interface	High Level	I²C Address (7bit)
Real Time Clock	PCF8523	I2C4	3.3 V	0x68
PCIe Clock Generator	SI52144	I2C4	3.3 V	0x6B
PMIC1	DA9063L	I2C5	1.8 V	0x5A
PMIC2	DA9210	I2C5	1.8 V	0x68

The interfaces at the emCON connector operate with 400 kHz clock and have 2K2 pull-up resistors to 3.3 V.

The pins of the interface I2C1 at the emCON connector can also be driven by the IIC1 controller of the RZ/G1M processor if needed.

3.14 SPI Interfaces

The RZ/G1M processor incorporates three SPI interfaces.

The interface MSIOF0 of the RZ/G1M processor is connected to the SPI1 interface of the emCON connector, the interface MSIOF1 is connected to the SPI2 interface.

Both SPI interface have CS1# and CS2# connected to MSIOFx_SS1# and MSIOFx_SS2#.

3.15 CAN

The RZ/G1M processor incorporates two CAN controllers, which comply with the ISO11898-1 specification. The CAN protocol specification 2.0B, with standard and extended message frames, are supported. The maximum baud rate is 1Mbps.

The TX and RX signals of both interfaces are routed to the emCON connector as LVTTL signals. CAN transceivers must be added externally.

3.16 General Purpose I/Os

The emCON interface provides eight dedicated GPIOs which are directly connected to the CPU. The following table shows the signal connections:

emCON Signal	RZ/G1M Pin	Direction
GPIO_1	GP4-13	In/Out
GPIO_2	GP4-14	In/Out
GPIO_3	GP4-15	In/Out
GPIO_4	GP4-16	In/Out
GPIO_5	GP4-17	In/Out
GPIO_6	GP4-18	In/Out
GPIO_7	GP4-19	In/Out
GPIO_8	GP4-20	In/Out

All signals have LVTTL level and can drive up to +/-4 mA when configured as output.

3.17 PWM

The RZ/G1M includes seven PWM timers. Three of them are used at the emCON connector:

emCON Signal	PWM Channel	Remark
LCD_BL_CTRL	PWM1	Backlight dimming
LVDS1_BL_CTRL	PWM2	Backlight dimming
PWM_FAN	PWM3	Fan control

The signal level of each PWM pin is 3.3V.

3.18 RTC

To enable time keeping while the module is powered off a RTC PCF8523 from NXP is fit. The RTC is connected to I^2C interface I2C4 of the RZ/G1M processor. The 7-bit I^2C address of the RTC is 0x68.

To keep the RTC running a voltage of minimum 1.5 V must be sourced at pin VBAT of the emCON connector. The battery current consumption of the RTC is below 0.5 µA.

3.19 Status LED

A bicolour LED is connected to the pins GP2_18 and GP2_19 of the RZ/G1M. If GP2_18 is high the LED is lighting green, if GP2-19 is high the LED is lighting red. If both pins are high the LED is lighting yellow.

An additional, green LED shows that the 3.3V supply is on.

3.20 Interrupts

The RZ/G1M processor has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor. The interrupts can be configured to be edge triggered on rising or falling edge or to be level sensitive on high or low level.

The emCON connector specifies six interrupt inputs. Two of them are reserved for touch interface controllers. Three inputs are generous interrupt inputs. The last interrupt input is provided as power fail input.

The following table shows the interrupt connections of the emCON connector:

Signal	RZ/G1M Pin
IRQ_1	**IRQ0**
IRQ_2	**IRQ1**
IRQ_3	**IRQ2**
IRQ_TOUCH1#	**IRQ3**
IRQ_TOUCH2#	**IRQ4**
POWERFAIL#	**NMI**

Additionally the PMICs drive in parallel the RZ/G1M interrupt pin IRQ5 locally on the module.

The interrupt inputs at the emCON connector are pulled high by 10 kΩ resistors.

3.21 Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the 3.3 V board supply voltage. If the voltage is too low a module reset is asserted. After the supply has risen above 2.93 V the reset is kept active for another 200 ms.
- If one of the other supply voltages fails the PMIC DA9063L drives reset low. The PMIC reset can also be caused by setting the SHUTDOWN bit in the PMIC DA9063L.
- The active low signal RESI# of the emCON connector causes a reset that is kept active for another 200 ms after RESI# became high.
- The signal JTAG_RESI# of the emCON connector directly causes a reset.
- A processor internal SW or Watchdog reset is also available.

All resets are hardware resets of the whole board.

The duration of the reset signal is min. 15ms. For resetting external devices the reset signal is available as an output (RESO#) at the emCON connector.

3.22 Power Supply

The power consumption of the module is 0.8 A – 2.5 A at +5V, +/- 5%. The current consumption depends on the software running.

All on board supply voltages that are required for the processor and the other components are generated on board by the two Power Management Chips DA9063L and DA9210 from Dialog Semiconductor.

The output voltages of the PMICs can be configured via the I^2C interface I2C5. The 7-bit I^2C address of the PMIC DA9063L is 0x5A, the 7-bit I^2C address of the PMIC DA9210 is 0x68.

3.22.1 Power Management Signals

VCC_5V, VCC_STANDBY

VCC_5V is the main supply input for the module. To keep only parts of the PMIC alive in power down states a second supply VCC_STANDBY is provided. This voltage only supplies parts of the PMIC DA9063L with little current consumption.

The output signal SUSPEND# of the emCON connector is provided to switch off the main supply VCC_5V in power down states. The switch must be realized on the carrier board. If no power management is needed, VCC_STANDBY and VCC_5V can be connected.

POWER_ON_BASE:

If the 3.3 V supply of the CPU module is switched off by power management, it must be ensured that no external peripherals with 3.3 V interface drive input pins. Otherwise unintended current flow might happen across the data lines.

The signal POWER_ON_BASE is provided to switch off external components with 3.3 V supply. The signal is high while the 3.3 V supply on the module is active. Otherwise the signal is low. The power switch must be realized on the carrier board.

POWERFAIL#

The signal POWERFAIL# is an input to signalize a power fail condition. The signal is connected to the NMI pin of the RZ/G1M processor.

ON_OFF#

The signal ON-OFF# can be used to switch the PMIC into power down and back to normal operating mode. This pin must be driven by an open collector circuit. A circuit on the module causes a low pulse every time when VCC_STANDBY powers up to cause an automatic start of the module.

BAT:

The pin BAT at the emCON connector is used as battery input for the RTC's backup power supply. The typical power consumption of the RTC at the BAT pin is < 0.5 µA.

4 emCON Interface

All interface signals of the board are available at the emCON connector.

The emCON interface is a 314 pos MXM connector. These sockets are available from various manufacturers.

The pin assignment is emtrion specific and match for the most needs of interfaces for actual embedded designs. Depending on the features of the CPUs every emtrion CPU module will use a subset of the emCON connector. More details can be found in emtrion's emCON specification.

Usage details of the connector and its electrical and mechanical characteristics can be found further down in this document.

Notes:

The pin assignment of the emCON connector is ONLY compatible with devices of emtrion's emCON-family. Insertion into a socket with another pin assignment may damage the emCON-RZ/G1M module and the carrier board.

Most of the pins are directly connected with the processor RZ/G1Mx.

5 Pin Assignments

5.1 J1, emCON Connector

Type MXM, 314 pos
Compatible carrier board connector: Aces 91782-3140M-001

Pin	Signal	Interface		Signal	Pin
1E20	GND	Power Supply		VCC_5V	2E20
1E19	GND			VCC_5V	2E19
1E18	GND			VCC_5V	2E18
1E17	GND			VCC_5V	2E17
1E16	GND			VCC_5V	2E16
1E15	GND			VCC_5V	2E15
1E14	GND			VCC_5V	2E14
1E13	GND			VCC_5V	2E13
1E12	GND			VCC_5V	2E12
1E11	GND			VCC_5V	2E11
1E10	BAT			VCC_STANDBY	2E10
1E9	n/c	Manufacturing	MISC	n/c	2E9
1E8	n/c			POWER_ON_BASE	2E8
1E7	n/c			IRQ_TOUCH1#	2E7
1E6	JTAG_RESET#			IRQ_TOUCH2#	2E6
1E5	JTAG_MOD			IRQ_1	2E5
1E4	JTAG_TRST#			IRQ_2	2E4
1E3	JTAG_TMS			IRQ_3	2E3
1E2	JTAG_TDO			RESO#	2E2
1E1	JTAG_TDI			RESI#	40
1	JTAG_RTCK			POWERFAIL#	2
3	1.8 V JTAG_VCC			SUSPEND#	4
5	JTAG_TCK			ON_OFF#	6
7	GND	POWER		n/c	8
9	UART-A_RXD	UART-A		PWM_FAN	10
11	UART-A_TXD		POWER	GND	12
13	UART-A_RTS		UART-C	UART-C_RXD	14
15	UART-A_CTS			UART-C_TXD	16
17	UART-B_RXD	UART-B	UART-D	UART-D_RXD	18
19	UART-B_TXD			UART-D_TXD	20
21	UART-B_RTS		UART-E	UART-E_RXD	22
23	UART-B_CTS			UART-E_TXD	24
25	GND	POWER		GND	26
27	GPIO_1	GPIOs	PCIe	n/c	28
29	GPIO_2			PCIE_RESET#	30
31	GPIO_3			PCIE_CLK1_P	32
33	GPIO_4			PCIE_CLK1_N	34
35	GPIO_5			GND	36
37	GPIO_6			PCIE_RX1_P	38

39	GPIO_7			PCIE_RX1_N	**40**
41	GPIO_8			PCIE_TX1_P	**42**
43	GND	**POWER**		PCIE_TX1_N	**44**
45	n/c			GND	**46**
47	n/c			n/c	**48**
49	n/c			n/c	**50**
51	n/c			n/c	**52**
53	n/c			n/c	**54**
55	n/c			GND	**56**
57	LCD_D17			n/c	**58**
59	LCD_D16			n/c	**60**
61	LCD_D15			GND	**62**
63	LCD_D14			n/c	**64**
65	LCD_D13			n/c	**66**
67	LCD_D12			n/c	**68**
69	GND			n/c	**70**
71	LCD_D11			GND	**72**
73	LCD_D10			n/c	**74**
75	LCD_D9	**RGB IF**		n/c	**76**
77	LCD_D8			n/c	**78**
79	LCD_D7			n/c	**80**
81	LCD_D6		**POWER**	GND	**82**
83	LCD_D5		**RFU**	n/c	**84**
85	LCD_D4			n/c	**86**
87	LCD_D3			n/c	**88**
89	LCD_D2			n/c	**90**
91	LCD_D1			n/c	**92**
93	LCD_D0			n/c	**94**
95	LCD_PIXCLK			n/c	**96**
97	LCD_HSYNC		**CPI2 Camera**	n/c	**98**
99	LCD_VSYNC			n/c	**100**
101	LCD_DISP			n/c	**102**
103	LCD_BL_CTRL			n/c	**104**
105	LCD_BL_EN			n/c	**106**
107	LCD_PANEL_EN			n/c	**108**
109	CAN2_RX	**CAN2**	**CAN1**	CAN1_RX	**110**
111	CAN2_TX			CAN1_TX	**112**
113	GND	**POWER**	**POWER**	GND	**114**
115	SPI1_SCK			SPI2_CS1#	**116**
117	SPI1_CS0#			SPI2_CS0#	**118**
119	SPI1_MOSI	**SPI 1**	**SPI 2**	SPI2_MOSI	**120**
121	SPI1_MISO			SPI2_MISO	**122**
123	SPI1_CS1#			SPI2_SCK	**124**
125	n/c				
	The pins 126 - 132 are used for mechanical coding and not available as electrical pins.				
133	CPI1_D0	**CPI1 Camera**	**MIPI_CSI2**	n/c	**134**

135	CPI1_D1		**Camera**	n/c	**136**
137	CPI1_D2			n/c	**138**
139	CPI1_D3			n/c	**140**
141	CPI1_D4			n/c	**142**
143	CPI1_D5			n/c	**144**
145	CPI1_D6			n/c	**146**
147	CPI1_D7			n/c	**148**
149	CPI1_CLK			n/c	**150**
151	CPI1_HSYNC			n/c	**152**
153	CPI1_VSYNC		**POWER**	GND	**154**
155	GND	**POWER**	**I2C1**	I2C1_SCL	**156**
157	LVDS1_BL_CTRL	**LVDS1 Control**		I2C1_SDA	**158**
159	LVDS1_BL_EN		**I2C2**	I2C2_SCL	**160**
161	LVDS1_PANEL_EN			I2C2_SDA	**162**
163	GND	**POWER**	**LVDS2**	n/c	**164**
165	LVDS1_D0_P	**LVDS1**		n/c	**166**
167	LVDS1_D0_N			n/c	**168**
169	LVDS1_D1_P			n/c	**170**
171	LVDS1_D1_N			n/c	**172**
173	LVDS1_D2_P			n/c	**174**
175	LVDS1_D2_N			n/c	**176**
177	LVDS1_D3_P			n/c	**178**
179	LVDS1_D3_N			n/c	**180**
181	LVDS1_CLK_P			n/c	**182**
183	LVDS1_CLK_N		**POWER**	GND	**184**
185	GND	**POWER**	**HDMI**	n/c	**186**
187	n/c	**SPDIF**		n/c	**188**
189	n/c			n/c	**190**
191	I2S_RXD	**I2S Audio**		n/c	**192**
193	I2S_TXD			n/c	**194**
195	I2S_TXFS			n/c	**196**
197	I2S_TXC			n/c	**198**
199	I2S_RXFS			n/c	**200**
201	I2S_RXC		**POWER**	GND	**202**
203	ACLK		**HDMI Control**	n/c	**204**
205	SATA_RX_P	**SATA**		n/c	**206**
207	SATA_RX_N			n/c	**208**
209	SATA_TX_P			n/c	**210**
211	SATA_TX_N		**POWER**	GND	**212**
213	GND	**POWER**		GND	**214**
215	USBOTG_ID	**USB OTG**	**USB Host**	USBH_D_P	**216**
217	USBOTG_D_P			USBH_D_N	**218**
219	USBOTG_D_N			n/c	**220**
221	USBOTG_VBUS			USBH_OC#	**222**
223	USBOTG_OC#			USBH_PEN#	**224**
225	USBOTG_PEN#		**USB3.0**	USBH_SSRX_P	**226**

227	n/c			USBH_SSRX_N	**228**
229	n/c		**POWER**	GND	**230**
231	GND	**POWER**	**USB3.0**	USBH_SSTX_P	**232**
233	n/c			USBH_SSTX_N	**234**
235	n/c		**POWER**	GND	**236**
237	GND	**POWER**	**SD Card 2**	SDC2_CLK	**238**
239	SDC1_CLK	**SD Card 1**		SDC2_CMD	**240**
241	SDC1_CMD			SDC2_D0	**242**
243	SDC1_D0			SDC2_D1	**244**
245	SDC1_D1			SDC2_D2	**246**
247	SDC1_D2			SDC2_D3	**248**
249	SDC1_D3			SDC2_CD#	**250**
251	SDC1_CD#			SDC2_WP	**252**
253	SDC1_WP		**POWER**	GND	**254**
255	GND	**POWER**	**Ethernet2**	n/c	**256**
257	GBE1_MDI0_P	**Ethernet1**		n/c	**258**
259	GBE1_MDI0_N			n/c	**260**
261	GBE1_MDI1_P			n/c	**262**
263	GBE1_MDI1_N			n/c	**264**
265	GBE1_MDI2_P			n/c	**266**
267	GBE1_MDI2_N			n/c	**268**
269	GBE1_MDI3_P			n/c	**270**
271	GBE1_MDI3_N		**POWER**	GND	**272**
273	GND	**POWER**	**Ethernet2**	n/c	**274**
275	GBE_1_LED_10_100#**	**Ethernet1**		n/c	**276**
277	GBE_1_LED_1000#**			n/c	**278**
279	GBE_1_TRAFFIC#			n/c	**280**
281	n/c				

** GBE_1_LED_1000# is shorted with GBE_1_LED_10_100#.

6 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	digital input
O	digital output
I/O	digital bidirectional
O(OD)	digital open drain output

PU xK	x KΩ pullup resistor
PD xK	x KΩ pulldown resistor
SR xR	x Ω series resistor
IPU xK	processor internal x KΩ pullup resistor
IPD xK	transistor internal x KΩ pulldown resistor
SC x	x Farad series capacitor

6.1 J1, emCON Connector

Name	RZ/G1M Pin	GPIO	Direction	Termination	Volt	Max. Current	Description
Gigabit Ethernet 1							
GBE1_MDI0_P			A I/O	-	-	N/A	GBE diff. data pair 0
GBE1_MDI0_N			A I/O	-	-	N/A	
GBE1_MDI1_P			A I/O	-	-	N/A	GBE diff. data pair 1
GBE1_MDI1_N			A I/O	-	-	N/A	
GBE1_MDI2_P			A I/O	-	-	N/A	GBE diff. data pair 2

GBE1_MDI2_N			A I/O	-	-	N/A	
GBE1_MDI3_P			A I/O	-	-	N/A	GBE diff. data pair 3
GBE1_MDI3_N			A I/O	-	-	N/A	
GBE1_LED_1000#			O	-	3.3V	20mA	Speed indication (GBE1_LED_1000# and GBE1_LED_10_100# are shorted)
GBE1_LED_10_100#			O	-	3.3V	20mA	Speed indication (GBE1_LED_1000# and GBE1_LED_10_100# are shorted)
GBE1_LED_TRAFFIC#			O	-	3.3V	20mA	Traffic indication
USB Host							
USBH_SSRX_P	AL27		I	-	SSTL	N/A	USB 3.0 super speed pair
USBH_SSRX_N	AL28		I	-	SSTL	N/A	
USBH_SSTX_P	AL29		O	SC 100n	SSTL	N/A	USB 3.0 super speed pair
USBH_SSTX_N	AL30		O	SC 100n	SSTL	N/A	
USBH_PEN#	AE28	GP7_25	O		3.3V	16mA	USB power enable
USBH_OC#	AD27	GP6_30	I	-	3.3V	N/A	USB overcurrent signal from power switch
USBH_DP	AJ31		I/O	-		N/A	USB 2.0 diff. data pair
USBH_DM	AK31		I/O	-		N/A	
USB OTG							
USBOTG_ID	AB31	GP2_25	I	PU 10K	3.3V	N/A	USB ID signal for OTG functionality
USBOTG_PEN#	AF31	GP7_23	O	-	3.3V	16mA	Host: USB power
USBOTG_OC#	AF30	GP7_24	I	PU 10K	3.3V	N/A	Host: USB overcurrent
USBOTG_VBUS	AF30	GP7_24	I	PD 10K	3.3V - 5V	N/A	Device: VBUS
USBOTG_DP	AG31		I/O	-		N/A	USB 2.0 diff. data pair
USBOTG_DM	AH31		I/O	-		N/A	

SATA							
SATA_TXP	AL25		A O	SC 12n	SSTL	N/A	SATA diff. data pair
SATA_TXN	AL26		A O	SC 12n	SSTL	N/A	
SATA_RXP	AL23		A I	SC 12n	SSTL	N/A	SATA diff. data pair
SATA_RXN	AL24		A I	SC 12n	SSTL	N/A	

PCIe							
PCIE_RXP	AL25		A I		SSTL	4mA	PCIe diff. data pair
PCIE_RXM	AL26		A I		SSTL	4mA	
PCIE_TXP	AL23		A O		SSTL	4mA	PCIe diff. data pair
PCIE_TXM	AL24		A O		SSTL	4mA	
CLK1_P			A O		SSTL	4mA	PCIe diff. clock pair
CLK1_N			A O		SSTL	4mA	
PCIE_RESET#	U31	GP7_7	O	PD 10K	3.3V	4mA	Reset output for PCIe

UART							
UART-A_TXD	P30	GP7_4	O	PU 10K	3.3V	4mA	UART transmit data
UART-A_RXD	P29	GP7_3	I		3.3V	N/A	UART receive data
UART-A_RTS	R25	GP7_1	O		3.3V	4mA	UART modem control
UART-A_CTS	P28	GP7_0	I		3.3V	N/A	UART modem control
UART-B_TXD	V26	GP7_6	O	PU 10K	3.3V	4mA	UART transmit data
UART-B_RXD	V25	GP7_5	I		3.3V	N/A	UART receive data
UART-B_RTS	U28	GP7_9	O		3.3V	4mA	UART modem control
UART-B_CTS	U29	GP7_8	I		3.3V	N/A	UART modem control
UART-C_TXD	T30	GP6_25	O		3.3V	4mA	UART transmit data
UART-C_RXD	T31	GP6_24	I		3.3V	N/A	UART receive data
UART-D_TXD	AB30	GP2_26	O	PU 10K	3.3V	4mA	UART transmit data
UART-D_RXD	AB29	GP2_27	I		3.3V	N/A	UART receive data

UART-E_TXD	R30	GP7_21	O		3.3V	4mA	UART transmit data
UART-E_RXD	R29	GP7_22	I		3.3V	N/A	UART receive data
CAN							
CAN1_TX	AK10	GP3_26	O		3.3V	4mA	CAN transmit data
CAN1_RX	AG8	GP3_29	I	PU 10K	3.3V	N/A	CAN receive data
CAN2_TX	R26	GP4_29	O		3.3V	4mA	CAN transmit data
CAN2_RX	R27	GP4_31	I	PU 10K	3.3V	N/A	CAN receive data
LCD (RGB Display)							
LCD_PIXCLK	AL10	GP3_25	O		3.3V	4mA	LCD dot clock
LCD_DISP	AH8	GP3_30	O		3.3V	4mA	LCD data enable signal
LCD_VSYNC	AF8	GP3_28	O		3.3V	4mA	LCD frame sync
LCD_HSYNC	AE8	GP3_27	O		3.3V	4mA	LCD line sync
LCD_D0	AG9	GP3_18	O		3.3V	4mA	LCD B2
LCD_D1	AF9	GP3_19	O		3.3V	4mA	LCD B3
LCD_D2	AE9	GP3_20	O		3.3V	4mA	LCD B4
LCD_D3	AJ10	GP3_21	O		3.3V	4mA	LCD B5
LCD_D4	AH10	GP3_22	O		3.3V	4mA	LCD B6
LCD_D5	AG10	GP3_23	O		3.3V	4mA	LCD B7
LCD_D6	AJ11	GP3_10	O		3.3V	4mA	LCD G2
LCD_D7	AH11	GP3_11	O		3.3V	4mA	LCD G3
LCD_D8	AG11	GP3_12	O		3.3V	4mA	LCD G4
LCD_D9	AF11	GP3_13	O		3.3V	4mA	LCD G5
LCD_D10	AF10	GP3_14	O		3.3V	4mA	LCD G6
LCD_D11	AE10	GP3_15	O		3.3V	4mA	LCD G7
LCD_D12	AJ12	GP3_2	O		3.3V	4mA	LCD R2
LCD_D13	AH12	GP3_3	O		3.3V	4mA	LCD R3
LCD_D14	AG12	GP3_4	O		3.3V	4mA	LCD R4

LCD_D15	AF12	GP3_5	O		3.3V	4mA	LCD R5
LCD_D16	AE12	GP3_6	O		3.3V	4mA	LCD R6
LCD_D17	AE11	GP3_7	O		3.3V	4mA	LCD R7
LCD_PANEL_EN	Y2	GP0_12	O		3.3V	4mA	LCD panel power enable
LCD_BL_EN	Y1	GP0_13	O		3.3V	4mA	LCD backlight power enable
LCD_BL_CTRL	V5	GP1_17	O		3.3V	4mA	LCD backlight brightness control
LVDS 1							
LVDS1_CLK_P	AE20		O		2,5V	2,5mA	LVDS diff clock pair
LVDS1_CLK_N	AF20		O		2,5V	2,5mA	
LVDS1_TX0_P	AJ23		O		2,5V	2,5mA	LVDS diff data pair
LVDS1_TX0_N	AJ22		O		2,5V	2,5mA	
LVDS1_TX1_P	AL21		O		2,5V	2,5mA	LVDS diff data pair
LVDS1_TX1_N	AL22		O		2,5V	2,5mA	
LVDS1_TX2_P	AJ20		O		2,5V	2,5mA	LVDS diff data pair
LVDS1_TX2_N	AJ21		O		2,5V	2,5mA	
LVDS1_TX3_P	AG22		O		2,5V	2,5mA	LVDS diff data pair
LVDS1_TX3_N	AG21		O		2,5V	2,5mA	
LVDS1_PANEL_EN	AA2	GP0_5	O	PD 2K2	3.3V	4mA	LVDS panel power enable
LVDS1_BL_EN	AA1	GP0_6	O	PD 2K2	3.3V	4mA	LVDS backlight power enable
LVDS1_BL_CTRL	N3	GP1_18	O		3.3V	4mA	LVDS backlight brightness control
CPI1 (Camera Input)							
CPI1_D0	AB4	GP4_5	I		3.3V	N/A	Video image input data
CPI1_D1	AB5	GP4_6	I		3.3V	N/A	Video image input data
CPI1_D2	AB6	GP4_7	I		3.3V	N/A	Video image input data
CPI1_D3	AC3	GP4_8	I		3.3V	N/A	Video image input data
CPI1_D4	AB7	GP4_9	I		3.3V	N/A	Video image input data
CPI1_D5	AC4	GP4_10	I		3.3V	N/A	Video image input data

CPI2_D6	AC6	GP4_11	I		3.3V	N/A	Video image input data
CPI1_D7	AC7	GP4_12	I		3.3V	N/A	Video image input data
CPI1_PIXCLK	AC1	GP4_0	I		3.3V	N/A	Video clock
CPI1_HSYNC	AB2	GP4_3	I		3.3V	N/A	Video line sync
CPI1_VSYNC	AB3	GP4_4	I		3.3V	N/A	Video frame sync
SD Card Interface 1							
SDC1_D0	AG16	GP6_2	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_D1	AF16	GP6_3	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_D2	AE16	GP6_4	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_D3	AH15	GP6_5	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC1_CMD	AH16	GP6_1	I/O	PU 47K	1.8V/3.3V	16mA	CMD signal
SDC1_CLK	AL15	GP6_0	O	SR 27R	1.8V/3.3V	16mA	SDC clock
SDC1_CD#	AJ15	GP6_6	I	PU 10K	3.3V	N/A	Card detect
SDC1_WP	AJ16	GP6_7	I	PD 10K	3.3V	N/A	Write protect
SD Card Interface 2							
SDC2_D0	SD2_D0	GPIO1-15	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_D1	SDC_D1	GPIO1-14	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_D2	SD2_D2	GPIO1-13	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_D3	SD2_D3	GPIO1-12	I/O	PU 47K	1.8V/3.3V	16mA	SDC data
SDC2_CMD	SD2_CMD	GPIO1-11	I/O	PU 47K	1.8V/3.3V	16mA	CMD signal
SDC2_CLK	SD2_CLK	GPIO1-10	O	SR 27R	1.8V/3.3V	16mA	SDC clock
SDC2_CD#	GPIO_4	GPIO1-4	I	PU 10K	3.3V	N/A	Card detect
SDC2_WP	GPIO_2	GPIO1-2	I	PD 10K	3.3V	N/A	Write protect
SPI1							
SPI1_SS0#	W6	GP0_18	O		3.3V	4mA	SPI slave select
SPI1_SS1#	W5	GP0_19	O		3.3V	4mA	SPI slave select
SPI1_SCK	T7	GP0_16	O		3.3V	4mA	SPI clock
SPI1_MISO	W3	GP0_21	I		3.3V	N/A	SPI data from slave

SPI1_MOSI	W4	GP0_20	O		3.3V	4mA	SPI data to slave
SPI2							
SPI2_SS0#	T5	GP0_24	O		3.3V	4mA	SPI slave select
SPI2_SS1#	T4	GP0_25	O		3.3V	4mA	SPI slave select
SPI2_SCK	T6	GP0_22	O		3.3V	4mA	SPI clock
SPI2_MISO	T3	GP0_27	I		3.3V	N/A	SPI data from slave
SPI2_MOSI	V6	GP0_26	O		3.3V	4mA	SPI data to slave
I2C1							
I2C1_SCL	V28	GP2_4	I/O	PU 2K2	3.3V	3mA	I^2C clock
I2C1_SDA	V27	GP2_5	I/O (OD)	PU 2K2	3.3V	3mA	I^2C data
I2C2							
I2C2_SCL	W30	GP2_6	I/O	PU 2K2	3.3V	3mA	I^2C clock
I2C2_SDA	W29	GP2_7	I/O (OD)	PU 2K2	3.3V	3mA	I^2C data
Audio SSI							
AUDIO_RXD	Y29	GP2_14	I		3.3V	N/A	Audio input data
AUDIO_TXD	W25	GP2_11	O		3.3V	4mA	Audio output data
AUDIO_TXC	Y31	GP2_12	I/O		3.3V	4mA	Audio transmit bit clock
AUDIO_TXFS	Y30	GP2_13	I/O		3.3V	N/A	Audio transmit frame select
AUDIO_RXC	W27	GP2_9	I/O		3.3V	4mA	Audio receive bit clock
AUDIO_RXFS	W26	GP2_10	I/O		3.3V	N/A	Audio receive frame select
ACLK	AD31	GP2_28	I		3.3V	4mA	Audio master clock
General Purpose I/O							
GPIO1	AD1	GP4_13	I/O		3.3V	4mA	digital input / output
GPIO2	AD2	GP4_14	I/O		3.3V	4mA	digital input / output
GPIO3	AD3	GP4_15	I/O		3.3V	4mA	digital input / output
GPIO4	AD4	GP4_16	I/O		3.3V	4mA	digital input / output

GPIO5	AD5	GP4_17	I/O		3.3V	4mA	digital input / output
GPIO6	AD6	GP4_18	I/O		3.3V	4mA	digital input / output
GPIO7	AE6	GP4_19	I/O		3.3V	4mA	digital input / output
GPIO8	AD7	GP4_20	I/O		3.3V	4mA	digital output only
Manufacturing							
JTAG_TCK	AE18		I	PU 10K	1.8V	N/A	JTAG clock (JTAG_TCK and JTAG_RTCK are shorted)
JTAG_TMS	AF18		I	PU 10K	1.8V	N/A	JTAG mode select
JTAG_TRST#	AF19		I	PD 1K	1.8V	N/A	JTAG test reset
JTAG_TDI	AH17		I	PU 10K	1.8V	N/A	JTAG data input
JTAG_TDO	AJ17		O		1.8V	1mA	JTAG data output
JTAG_RTCK	AE18		O	PU 10K	1.8V	N/A	JTAG return clock (JTAG_TCK and JTAG_RTCK are shorted)
JTAG_MOD	R7	GP0_29	I		3.3V	N/A	Mode selection JTAG/Boundary Scan
JTAG_RESET#					1.8V	N/A	JTAG reset
JTAG_VCC					1.8V		JTAG voltage reference
Miscellaneous							
IRQ_1	AE30	GP7_10	I	PU 10K	3.3V	N/A	Interrupt input
IRQ_2	AE29	GP7_11	I	PU 10K	3.3V	N/A	Interrupt input
IRQ_3	AD29	GP7_12	I	PU 10K	3.3V	N/A	Interrupt input
IRQ_TOUCH1#	AD28	GP7_13	I	PU 10K	3.3V	N/A	Interrupt input for touch controller
IRQ_TOUCH2#	AC29	GP7_14	I	PU 10K	3.3V	N/A	Interrupt input for touch controller
POWERFAIL#	AL16		I	PD 20K	5V	N/A	Power Fail interrupt
PWM_FAN	U4	GP1_24	O		3.3V	5mA	PWM signal for fan control
RESI#			I	PU 10K	3.3V	N/A	Reset input from carrier board
RESO#			O		3.3V	20mA	Reset output to carrier board
POWER_ON_BASE			O		3.3V	20mA	Power enable signal for the

					3.3V baseboard supply
SUSPEND#	O		3.3V	20mA	Power switching signal for VCC_5V
ON_OFF#	I	PU 100K	5V	N/A	Power management signal
Power Supply					
BAT	-	-	1.5V – 3.3V	N/A	Battery backup supply for RTC
VCC_5V	-	-	-	N/A	+ 5V supply
VCC_STANDBY	-	-	-	N/A	+ 5V standby supply
GND	-	-	-	N/A	Ground

7 Technical Characteristics

7.1 Electrical Specifications

Supply voltage	5V, +/-5%
Current consumption	up to 2.5 A

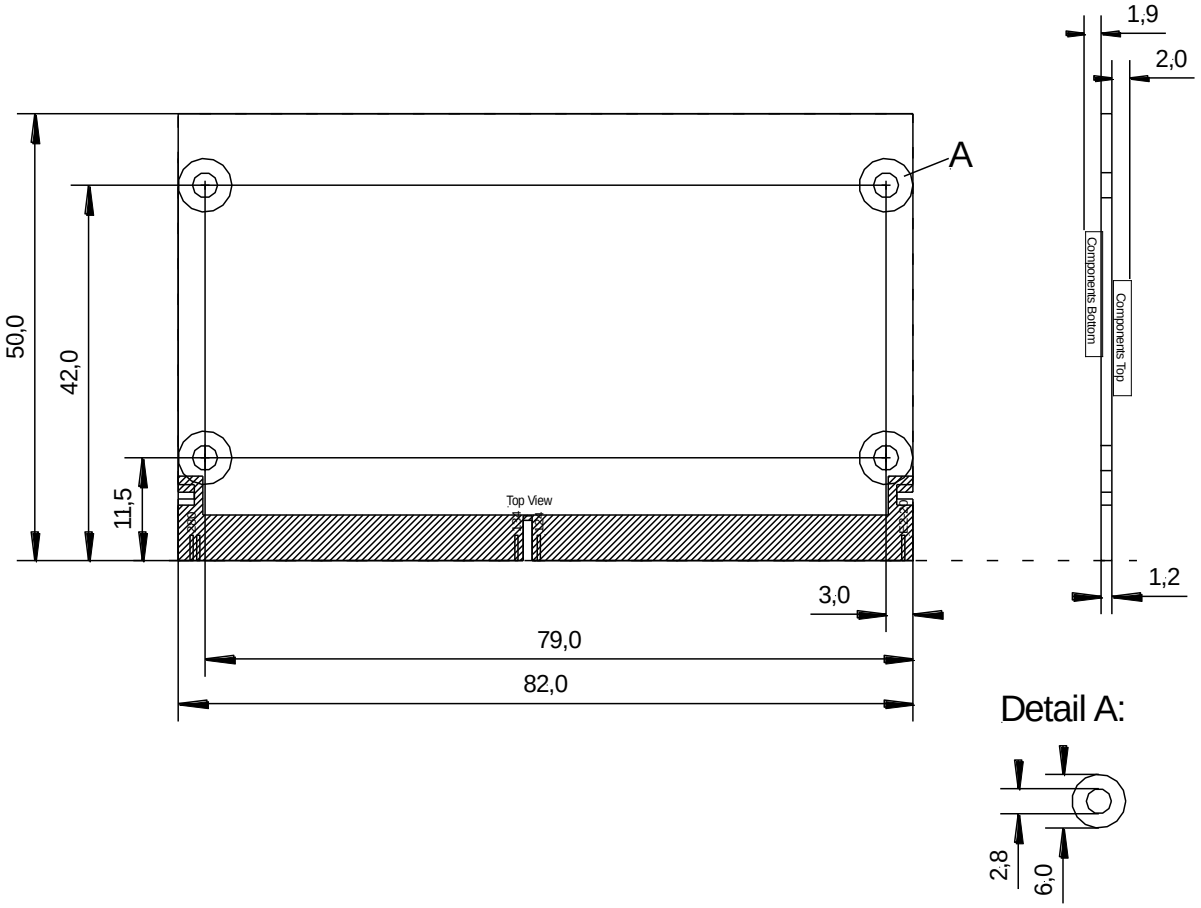
7.2 Environmental Specifications

Operating temperature Standard: Extended: **Storage temperature**	 0 ... +70°C -40 ... +85°C -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

7.3 Mechanical Specifications

Weight	approx. 19 g
Board	Glasepoxi FR-4, UL-listed, 10 layers
Dimensions	82.2 mm x 50.0 mm x 5.0 mm

8 Dimensional Drawing



9 References

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