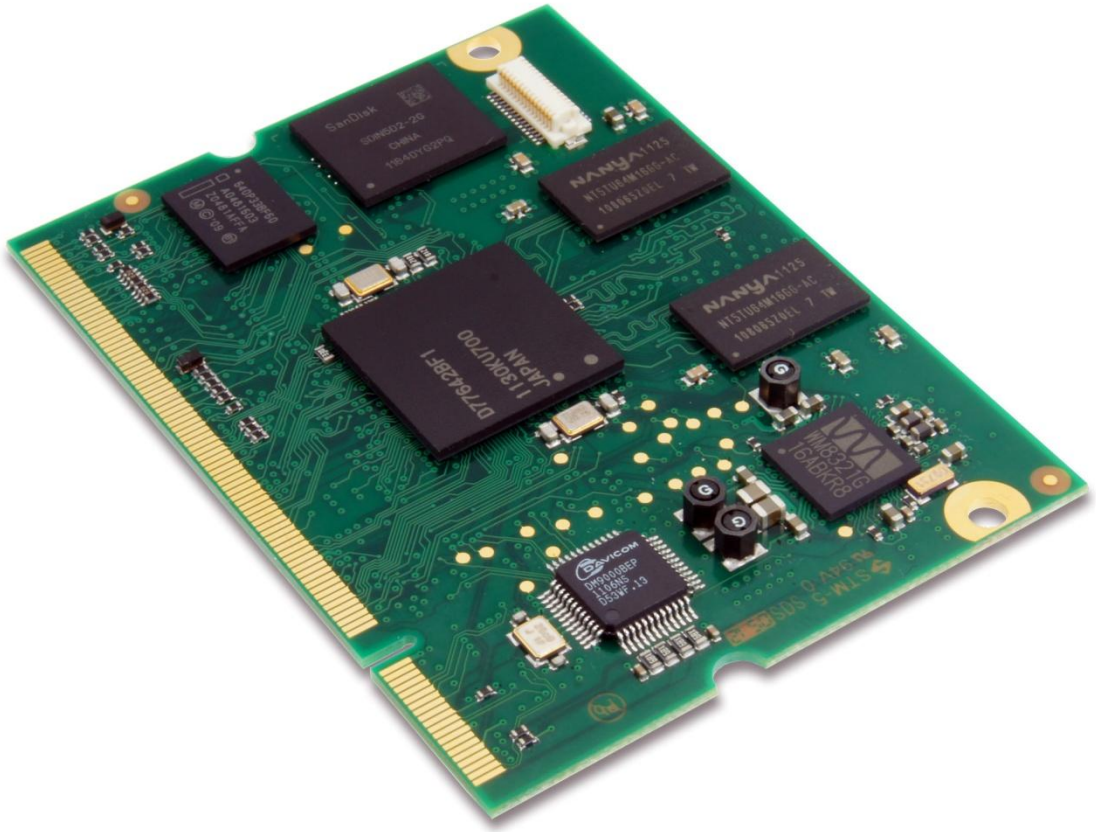
DIMM-EMEV2

Hardware Manual

Rev1 / 21.03.2012



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1 Introduction

The DIMM-EMEV2 processor module is a SODIMM sized CPU board based on the processor EM/EV2 from Renesas. The EM/EV2 processor is part of the EMMA family from Renesas which is an acronym for Enhanced Multi Media Architecture.

EM/EV2 utilizes two ARM® Cortex-A9 cores with two Neon extensions running at 533 MHz. It includes a variety of functions required for multimedia or industrial applications. An audio video engine and a 3D graphics block enable high-class processing in a range of applications. Interfaces for camera, displays, mass storage devices, memory devices and many other peripherals are integrated in the processor.

The CPU is accompanied by up to 512 MB DDR2 SDRAM, 32 MB NOR flash, 2 GB eMMC, 100Base-TX Ethernet and CAN interface to the CPU. Also an integrated power management controller is added.

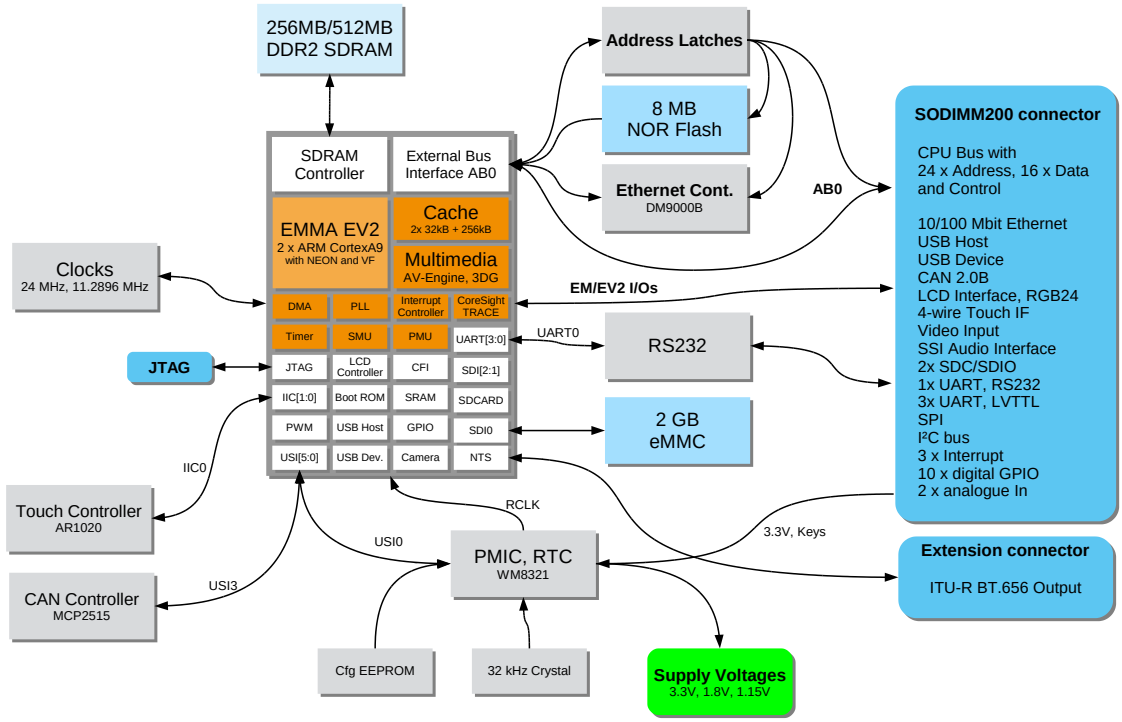
All interfaces are accessible through a 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2.5V keying and an additional extension connector.

The following table summarizes the main features and interfaces of the DIMM-EMEV2 module:

DIMM-EMEV2
256/512MB DDR2 SDRAM
8 MB NOR Flash
2 GB eMMC
10/100Mbit Ethernet
USB 2.0 Host
USB 2.0 Device
LCD Interface 16/18/24bit max. 1080p (1920 x 1080)
ITU-R BT.656 video output
ITU-R BT.656 Video In
4 wire resistive Touch
SSI Audio
1 x UART RS232
3 x UART LVTTL
CAN V2.0B
SD Card interface
SDIO interface
SPI
I^2C
Processor bus with16 bit data, 24 bit address, 2 chip selects, 3 interrupts
10 x digital IO, 2 x analog In
RTC
JTAG interface
3.3V supply
Operating temperature range -10°C to 70°C

2 Block Diagram

The following figure shows the block diagram of the DIMM-EMEV2.



3 Handling Precautions

Please read the following notes prior to installing the DIMM-EMEV2 processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The DIMM-EMEV2 does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The DIMM-EMEV2 module is based on the processor EM/EV2 from Renesas. It utilizes two ARM® Cortex-A9 cores with Neon extensions running at 533MHz.

In addition to the CPU cores with MMU, FPU and Caches, the processor provides a lot of multimedia function features, memory interfaces and peripheral function blocks:

- The video decoder that can perform H.264, VC-1 and MPEG-4 decoding. It supports up to Full HD resolution (1920 x 1080) @ 30 fps and can decode multiple video clips that use multiple standards simultaneously.
- The audio decoder that can decode data in the following formats: WMA, MP3, MPEG-4, HE-AAC and enhanced aacPlus.
- The rotator is a macro that is used to rotate an image by multiples of 90°.
- The resizer is a macro used to resize or rotate an image.
- The image composer generates a synthesized image from source images of several layers. Alpha-bending, gamma correction and colour format transfer YUV to RGB are supported. The output is directly driven to the LCD interface.
- With the PowerVR 3D graphics accelerator core 14.7 Mpoly/s 3D performance, 500 Mpixels/s 2D performance and 1.6 GFLOPS shader performance are achievable. The API is OpenGL-ES 2.0 and OpenVG 1.1 compatible.

- LCD interface up to 1080p (1920 x 1080) and 16/18/24 bpp, RGB or YUV interface
- ITU-R BT.656 video output according to NTSC or PAL standard
- Camera capture interface with up to 16 Mpixels resolution

- DDR2 SDRAM controller
- Processor Bus Controller with SRAM and NOR Flash interface
- Memory card interfaces, 2 x SDIO, 1 x SDC
- Serial interfaces including USB 2.0 host, USB 2.0 device, 4 x UART, I^2C, 6 x USI programmable as either SPI or sound interface

- DMA controller
- Interrupt controller
- 15 channel interval timer
- Various GPIOs

- Power management unit
- Internal memories: 128 kB SRAM and 64 kB ROM containing bootloader
- JTAG debug interface

Further details of the processor can be found in the EMMA Mobile EV1/2 hardware manuals [1].

4.1.1 Processor Clocks

Most of the processor's internal clocks are derived from a 32.768 kHz clock supplied by PMIC. This clock is multiplied by four PLLs inside the CPU.

PLL1 can be programmed to 400 – 533 MHz. It is used as internal system clock. PLL2 is unused. PLL3 is operating at the fixed frequency 229.376 MHz. It is used as clock source for most integrated peripherals. The CPU is clocked at 533 MHz from PLL4. The SDRAM interface is operated at 266 MHz by PLL4/2.

Two further crystals are connected to the processor. An 11.2896 MHz crystal is connected to OSC0. It is used as audio clock source (44.1 kHz * 256). A 24 MHz crystal is connected to OSC1. It is used as clock source for the USB interfaces. OSC0 and OSC1 can also be used as clock source for the CPU in power down states.

The clock input EXT_CLKI is connected to the NTSC extension connector. A 27 MHz clock must be provided from the carrier board to use the NTSC interface.

4.1.2 Boot Mode

The DIMM-EMEV2 can either boot from the NOR flash, eMMC or from an SD card. The boot mode is selected via two DIP Switches SW1-x:

SW1-2	SW1-1	Boot device
off	**off**	not valid
off	**on**	eMMC
on	**off**	SD card
on	**on**	NOR flash

Please watch that an SD card socket is not available on the DIMM-EMEV2 module. It has to be added externally. Also the card must be formatted and contain adopted boot files.

(Please contact emtrion GmbH)

4.1.3 Interrupts

The processor EM/EV2 incorporates an integrated ARM Generic Interrupt Controller, GIC, which has 166 Interrupt sources. The GIC monitors all interrupt sources, prioritize them and outputs the interrupt with the highest priority to the CPU.

Seven GPIO pins provide unique interrupt inputs for onboard peripherals and external chips connected at the SODIMM connector.

GPIO Pin	Interrupt	Source
GPIO_000	GIO0_INT	PMIC
GPIO_016	GIO1_INT	Ethernet Controller DM9000B
GPIO_049	GIO3_INT	CAN Controller MCP2515
GPIO_106	GIO6_INT	Touch Controller AR1020
GPIO_114	GIO7_INT	SODIMM NMI

GPIO_143	GIO8_INT	SODIMM IRQ-A
GPIO_144	GIO9_INT	SODIMM IRQ-B

The signalling level of all interrupts is 3.3V.

4.2 NOR-Flash

An 8 MByte NOR flash of type 28F640P33B85 from Micron is used. It is connected to the processor bus interface at CS0# at therefore addressed in the address range 0x0000_0000 – 0x007F_FFFF.

The integrated bootloader of the processor supports booting from the NOR flash. This can be configured by DIP switches SW1-x.

Write protection of the NOR flash is realized by two port pins of the processor:

- The write protect input WP# of the NOR Flash is connected with GPIO_024.
- The voltage V_{PPL} of the NOR Flash is controlled by GPIO_019.

The following table shows the protection mode according to the GPIO values:

GPIO_024 [WP#]	GPIO_019 [VPPL]	Write Protection
0	**0**	All blocks are write protected
0	**1**	Only locked blocks are write protected
1	**0**	All blocks write protected
1	**1**	No write protection

Both GPIOs have integrated pull-downs which are active during reset and standby. This ensures full write protection of the Flash in power down states of the CPU.

For special applications, the NOR Flash size can be increased up to 32 MByte. (Please contact emtrion GmbH)

4.3 eMMC

A 2 GByte eMMC which is based on MLC NAND flash cells is connected to the SDIO0 interface of the processor. The interface is compatible to the MMC/eMMC System Spec. Ver. 4.2.

The integrated bootloader of the processor supports booting from the eMMC. This can be configured by DIP switches SW1-x.

The eMMC chip is connected by an 8 bit wide data bus and supports up to 25 MHz clock. Therefore up to 25 MByte/s transfer rate can be achieved at the eMMC interface.

The capacity of the eMMC can be increased if needed. (Please contact emtrion GmbH)

4.4 DDR2 SDRAM

256 MByte or 512 MB DDR2 SDRAM are available as main memory. The 256MB memory consists of two 1Gbit DDR2 SDRAM, type 64M x 16. The 512MB memory consists of two 2Gbit DDR2 SDRAM, type 128M x 16. They are clocked at 266 MHz and accessed with CAS latency 4.

256 MB RAM is located in the address range 0x4000_0000 … 0x4FFF_FFFF. 512MB RAM is located in the address range 0x4000_0000 … 0x5FFF_FFFF.

4.5 Processor Bus Interface

The AB0 processor bus interface of the CPU EM/EV2 is available at the SODIMM connector. It consists of a 16 bit wide data bus with 24 bit address lines. External memory or peripheral chips with SRAM type interface can be connected to this bus interface.

Watch that the CPU does not support byte accesses! Therefore address pin A0 of the SODIMM connector is connected to GND and only 16 bit accesses to even addresses are allowed.

A 66 MHz bus clock, read and write control signals, 2 chip select signals and WAIT# input are also routed to the SODIMM connector. All signal levels are LVTTL compatible.

The chip select CS1# is active in the range 0x2800_0000 … 0x280F_FFFF. The chip select CS2# is active in the range 0x2810_0000 … 0x281F_FFFF. The address ranges and individual timing of the read and write control lines can be programmed for both chip select areas by software.

The following table describes the processor bus interface signals:

Signal	Description
A[23:1]	Address bus, A0 = 0
D[15:0]	Data bus
CKIO	66 MHz bus clock
WAIT#	active low wait input
CS1#	active low active chip select 1
CS2#	active low active chip select 2
RD#	active low read control signal
WE0#	active low write control signal
WE1#	same as WE0#
BS#	active low pulse at start of bus cycle
NMI	interrupt GIO7
IRQ-A	interrupt GIO8
IRQ-B	interrupt GIO9

Please contact emtrion GmbH for further information.

4.6 Ethernet

The Ethernet interface is realized with an Ethernet controller DM9000B from Davicom [2]. This controller comprises the Media Access Controller (MAC) and the Physical Layer Interface (PHY) in a single chip.

An integrated 16 KByte on-chip SRAM serves to buffer transmit- and receive frames. The chip is able to adapt itself to the operating modes 100BASE-TX and 10BASE-T, both half- and full duplex. Also HP Auto-MDIX is supported.

The Ethernet controller is connected to the processor bus interface AB0 using CS1#. Only two addresses are needed. The index port is located at address 0x2000_0000 and the data port at 0x2000_0002. The interrupt output of the Ethernet controller is connected to GPIO_016. This causes a GIO1 interrupt.

The Ethernet signal line pairs ETH_TDP/ETH_TDM and ETH_RDP/ETH_RDM as well as two status signals SPEED_LED# and LINK_LED# are connected to the SODIMM connector.

The signal LINK_LED# indicates if data packages are transferred. If a link is established every packet causes an 80 ms long low pulse.

The signal SPEED_LED# indicates the transfer speed of the connection. Low = 100 Mbit/s, high = 10 Mbit/s.

A 1:1 transformer with centre taps connected to 1.8V, must be added externally to the signal lines.

4.7 USB Host

A USB Rev 2.0 compliant host interface is integrated in the processor EM/EV2. The registers of the USB host conform to the OHCI/EHCI standard. High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) transfers are supported.

The data line pair USBH_DP/USBH_DM is available at the SODIMM connector. The lines are terminated on-board with 15-KΩ pull-down resistors.

A VBUS power switch must be added externally. The power switch control output USBH_PEN# and the overcurrent signal input USBH_OC# are realized by GPIO pins. GPIO_007 controls enable of the VBUS switch. A logical “0” switches the power on; a logical “1” turns the power off. GPIO_008 serves as overcurrent input. A logical “0” signal overcurrent. Both GPIOs have Hi-Z state during reset and standby. Pull-up resistors keep the signals high during that time.

4.8 USB Device

A USB Rev 2.0 compliant device interface is integrated in the processor EM/EV2. High-Speed and Full-Speed transfers are supported.

The data line pair USBF_DP/USBF_DM is available at the SODIMM connector. The VBUS input USBF_VBUS is also available at the SODIMM connector. USBF_VBUS is only used to signal that a Host is connected. Now power is drawn from VBUS.

The USB device port allows data transmission to an external host, for example a Host PC.

4.9 LCD Interface and Video Output

4.9.1 General

The processor EM/EV2 includes an integrated LCD controller that supports two different output formats. Either RGB data are output to drive a TFT LCD display or YUV data are output to realize a HDMI interface.

The LCD controller can drive displays with resolutions up to 1080p (1920 x 1080). The RGB colour depth can be 16/18/24bpp, YUV output is always YUV422 format. The control signals HSYNC, VSYNC and DATAENABLE are driven based on the pixel clock. The pixel clock is generated internally or can be sourced via the SODIMM connector pin LCD_LCLK. Thus all timings can individually be adapted to the connected display.

Two GPIO output signals can be used to control the power supply of a display.

Signal	Description
LCD_VEPWC	Optional display power control output, driven by GPIO_009
LCD_VCPWC	Optional display power control output, driven by GPIO_010

All data and control lines are available at the SODIMM connector.

4.9.2 LCD interface

The following table describes the function of the data and control lines in RGB mode.

Signal	Description
LCD_D[23:0]	Colour data, mapping according to the following table
LCD_VSYNC	Vertical synchronization signal
LCD_HSYNC	Horizontal synchronization signal
LCD_DISP	Data enable signal signaling active data
LCD_DCK	Pixel clock output
LCD_LCLK	External input clock for LCD interface (e.g. spread spectrum oscillator). The maximum input clock is 90 MHz.
LCD_DON	Display power enable signal. Used to switch the backlight power (“0” backlight off; “1” backlight on)

The following table shows the RGB colour mapping of the LCD_D[23:0] pins at the SODIMM connector depending on the colour depth:

LCD_D[23:0]	RGB565 (16bit)	RGB666 (18bit)	RGB888 (24bit)
LCD_D0	always low	B0	B2
LCD_D1	B0	B1	B3
LCD_D2	B1	B2	B4
LCD_D3	B2	B3	B5
LCD_D4	B3	B4	B6
LCD_D5	B4	B5	B7
LCD_D6	G0	G0	G2
LCD_D7	G1	G1	G3
LCD_D8	G2	G2	G4
LCD_D9	G3	G3	G5
LCD_D10	G4	G4	G6
LCD_D11	G5	G5	G7
LCD_D12	always low	R0	R2
LCD_D13	R0	R1	R3
LCD_D14	R1	R2	R4
LCD_D15	R2	R3	R5
LCD_D16	R3	R4	R6
LCD_D17	R4	R5	R7
LCD_D18	-	-	B0
LCD_D19	-	-	B1
LCD_D20	-	-	G0
LCD_D21	-	-	G1
LCD_D22	-	-	R0
LCD_D23	-	-	R1

Watch that the lower 18 data lines LCD_D[17:0] always drive the upper 18 colour bits with 6 bpp. In RGB565 mode blue and red have only 5 bits and therefore the lowest bit is always 0. In RGB888 mode the two lowest bits of each colour are available at LCD_D[23:18].

This pin routing was realized to be compatible to other DIMM modules of emtrion.

4.9.3 YUV Interface

The following table describes the function of the data and control lines in YUV mode.

Signal	YUV Signal	Description
LCD_D[23:0]	YUV_D[15:0]	Colour data according to following table
LCD_VSYNC	VUY_VS	Vertical synchronization signal
LCD_HSYNC	YUV_HS	Horizontal synchronization signal
LCD_DISP	YUV_DE	Data enable signal signaling active data
LCD_DCK	YUV_CLK	Pixel clock output
LCD_LCLK		External input clock for LCD interface (e.g. spread spectrum oscillator)

The following table shows the YUV colour mapping of the LCD_D[23:0] pins at the SODIMM connector:

LCD_D[23:0]	YUV Data
LCD_D0	D10
LCD_D1	D11
LCD_D2	D12
LCD_D3	D13
LCD_D4	D14
LCD_D5	D15
LCD_D6	D2
LCD_D7	D3
LCD_D8	D4
LCD_D9	D5
LCD_D10	D6
LCD_D11	D7
LCD_D12	-
LCD_D13	-
LCD_D14	-
LCD_D15	-
LCD_D16	-
LCD_D17	-
LCD_D18	D8
LCD_D19	D9
LCD_D20	D0
LCD_D21	D1
LCD_D22	-
LCD_D23	-

Watch that only the LCD interface output is supported at the DIMM-Base boards Lothron and Verno from emtrion

4.10 ITU-R BT.656 Video output

Besides the YUV output of the LCD controller a special video output interface is available. The controller fetches YUV422-format image data from a frame buffer memory, converts them and outputs them to an ITU-R BT.656 compliant interface. This output can be connected to an external NTSC/PAL encoder chip.

The video output signals are connected to an extension connector which is compatible to the carrier board DIMM-Base-Lothron from emtrion.

The output signal VOU_RST# is also available at the SODIMM connector. This signal is driven by GPIO_028 and by the board reset signal and can be used to reset an external video encoder.

4.11 Touch Interface

A 4-wire resistive touch interface is implemented by using the AR1020 touch interface controller from Microchip [3].

The controller is connected to the I^2C bus interface IIC0 of the EM/EV2. The pen interrupt output of the controller causes GIO_06 interrupts. It is also connected to GPIO4 of the PMIC to support wakeup by touch events.

The 7-bit I^2C-Address of the AR1020 is 0x4D.

The 4 touch interface signals TOUCH_XP, TOUCH_XM, TOUCH_YP and TOUCH_YM are available at the SODIMM connector.

4.12 Video Input

The DIMM-EMEV2 has a video input unit which can be used to connect a CMOS camera with up to 16 Mpixels resolution.

The interface uses an 8-bit wide data bus. All data and control signals are available at the SODIMM connector. The following table describes the video input signals.

Signal	Description
VIO_D[7:0]	Video input data
VIO_CLK	Video input clock
VIO_CKO	Video output clock
VIO_HD	Video input horizontal synchronization
VIO_VD	Video input vertical synchronization

On the carrier board DIMM-Base-Lothron from emtrion the video source can be switched between a video codec output and a CMOS camera connector. To switch between the two video sources the signal VIO_SRC is available at the SODIMM connector. The signal is driven by GPIO_017.

Additionally the output signal VIO_RST# is available at the SODIMM connector. This signal is driven by GPIO_006 and by the board reset signal. It can be used to reset an external video decoder.

Signal	Description
VIO_SRC	Video input source selection; “0” = CMOS camera; “1” = video decoder
VIO_RST#	Video input source reset; “0” = reset; “1” = normal operation

4.13 Audio Interface

The serial interface USIA-S1of the processor EM/EV2 is operated as IIS audio interface to connect an external audio codec. The interface can be operated in master or slave mode.

Independent of the audio interface settings an 11.2896 MHz reference clock can be driven at the pin AUDIO_MCLK of the SODIMM connector. The frequency is 256 * 44.1 kHz.

The interface signal lines are connected to SODIMM connector.

4.14 CAN Controller

Since the processor EM/EV2 does not incorporate a CAN interface it is realized by a CAN controller MCP2515 from Microchip [4]. This chip has the following characteristics:

- supports CAN specification V2.0B
- up to 1Maud transfer rate
- 0-8 byte data length
- two receive buffers with prioritization
- three transmit buffers with prioritization

The controller is connected to the USIB-S3 interface of the EM/EV2. The interrupt output causes GIO3 interrupts. The CAN controller is clocked by a 24 MHz crystal.

The CAN controllers data signal lines are available with TTL level at the SODIMM connector. An appropriate CAN transceiver must be added externally.

4.15 SD-Card and SDIO Interface

The EM/EV2 processor includes an SD card controller and two SDIO controllers.

The interface pins of the SD card controller and the pins of one SDIO controller are connected to the SODIMM connector so that a socket can be connected directly.

Card detect and write protect inputs for both interfaces are also provided. They are realized by GPIO pins.

4.16 Serial Ports

The processor EM/EV2 contains four TL16C750 compatible UARTs which incorporate 64 Byte FIFOs. The baud rates of all UARTs are generated by dividing the internal 229.376 MHz clock.

UART0 is used as terminal interface and therefore an RS232 transceiver like MAX3221E is connected to UART0 on the DIMM module. The RS232 transceiver is disabled after reset. By programming GPIO_025 to drive a high level the RS232 transceiver is enabled. The RS232 signals are routed to the SODIMM connector.

The signals of UART1, UART2 and UART3 are connected directly as LVTTL signals to the SODIMM connector. Only UART1 provides RTS/CTS flow control pins which are multiplexed with the data signals of UART2.The following table shows the UART connections:

SODIMM interface	EM/EV2 interface	Signal level
UART_A	UART0	RS232
UART_B	UART1	LVTTL
UART_C	UART2 (or optional UART1 RTS/CTS)	LVTTL
UART_D	UART3	LVTTL
UART_E	not used	-

4.17 I²C- Bus

The EM/EV2 provides an I²C bus interface with transmission speeds up to 383 kb/s. The interface is operated in master mode. It is used for the touch controller AT1020 on the DIMM module and available at the SODIMM connector for external extensions.

The SCL and SDA lines are pulled up with 2.2 kΩ resistors to 3.3V.

4.18 SPI Interface

The USIB-S2 interface of the EM/EV2 is available as SPI interface at the SODIMM connector. The characteristics of the interface can be individually controlled by software.

4.19 Digital and Analog I/Os

10 digital GPIOs for individual use are available at the SODIMM connector. They have the following meaning:

SODIMM Pin	Signal
GPIO_0	reserved, do not use
GPIO_1	PMIC, GPIO5 (Wakeup)
GPIO_2	EM/EV2, GPIO_029
GPIO_3	EM/EV2, GPIO_015
GPIO_4	EM/EV2, GPIO_120 (PWM0)
GPIO_5	EM/EV2, GPIO_121 (PWM1)
GPIO_6	EM/EV2, GPIO_031
GPIO_7	EM/EV2, GPIO_030
GPIO_8	EM/EV2, GPIO_104
GPIO_9	EM/EV2, GPIO_102

The signal level of each GPIO pin is 3.3V. All pins are protected by 1 kΩ series resistors.

The signal at GPIO_0 is a dedicated input to switch the power supply of the DIMM module on. A low pulse which lasts longer than 1 s switches the supply on. By a local connection with reset the DIMM module switches on automatically.

The signal GPIO5 of the PMIC is provided to serve as wakeup input. A wakeup from power down states of the module can be established by appropriate software. Besides this the pin can also be used as general purpose input or output of the PMIC.

The signals GPIO_120 and GPIO_121 of the EM/EV2 can also be used as PWM outputs. This demands appropriate software.

Besides the digital I/Os two analogue inputs are available:

SODIMM Pin	Signal
ANA_IN1	PMIC, GPIO11
ANA_IN2	PMIC, GPIO12

The analogue inputs are connected with the PMIC pins GPIO11 and GPIO12. The voltage of these pins can be read by an integrated ADC with 12-bit resolution. The conversion time of the ADC is 39 µs. Input voltages must not exceed 3.3 V.

4.20 Status LED

A bicolour LED is located on the top side of the DIMM-EMEV2 module. This LED is normally used to signal the health state of the software.

After reset the LED shines red. After the bootloader has successfully started the LED shines green. The LED is controlled by the two LED outputs of the PMIC.

4.21 RTC

The PMIC incorporates a 32-bit counter which is clocked with 32.678 kHz. This counter is used as RTC. The counter clock can be buffered by an external battery connected to pin BAT of the SODIMM connector. The current consumption of the RTC circuit is about 3 µA.

4.22 Reset

There are several ways to reset the board:

- The PMIC supervises all voltages and causes a reset in undervoltage situations
- A low pulse at pin RESI# of the SODIMM connector
- A low signal at pin CSRSTZ# at the Debug connector
- The software can cause a reset by writing any value to register 0x0000 of the PMIC

All resets are hardware resets of the whole board.

To reset external devices the reset signal is driven to pin RESO# at the SODIMM connector.

4.23 Power Supply, PMIC

The maximum power consumption of the module DIMM-EMEV2 is 0.35 A at +3.3 V, +/- 5%. This voltage must be supplied via the SODIMM connector. All further voltages needed on the module are generated on board by the power management controller (PMIC) WM8321 from Wolfson Microelectronics [5].

The PMIC generates all voltages and cares about the appropriate voltage sequencing at power up. The voltages can be controlled by the processor EM/EV2 via the SPI interface USIA-S0. By this interface and some special control signals power management of the module is realized. A dedicated power on input is provided and a GPIO is reserved to cause wakeup events.

Besides the voltage regulators the PMIC incorporates a 32.768 kHz oscillator which supplies the clock for the processor and a 32-bit counter which is clocked by the same clock and is used as RTC. The clock and the counter can be buffered by an external battery.

The PMIC also contains an 12-bit ADC, which can measure several voltages and the chip temperature. Also a bicolour LED is controlled by the PMIC.

5 Connectors

5.1 Overview

The module DIMM-EMEV2 incorporates 3 connectors:

- SODIMM connector J1
- Debug connector J2
- Video Out extension connector J3

The picture in chapter 8.4 shows the view at the top side of the module. The odd contacts of J1 are at the top side, the even contacts are at the bottom side. J3 is located on the bottom side.

5.2 SODIMM connector

All interface signals of the board are available at the 200 pos SODIMM connector.

The connector complies mechanically to regular DDR1 SODIMM memory sockets with 2.5V keying. These sockets are available from various manufacturers.

Watch that the pin mapping of the SODIMM connector is NOT compatible with memory modules. Plugging the module into a socket with wrong pin out may damage the DIMM-EMEV2 and the carrier board.

5.3 Debug interface

All signals of the ARM debug interface are available at the 20 pin header J2.

Please contact emtrion GmbH for further details how to connect a JTAG tool to J2.

5.4 Video Out interface

The ITU-R BT.656 video out interface is available at the 30 pin extension connector J3. This connector is located at the bottom side of the board. It fits to the carrier board DIMM-Base-Lothron from emtrion.

6 Pin Assignments

6.1 J1, SODIMM

Type 200 pin SODIMM edge connector, 2.5V keying

Pin	Signal	Interface		Signal	Pin
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2
3	ETH_TDP			USBH_OC#	4
5	ETH_TDM			USBH_DM	6
7	GND			USBH_DP	8
9	ETH_RDP		USB Device	USBF_VBUS	10
11	ETH_RDM			USBF_DM	12
13	LINK_LED#			USBF_DP	14
15	n/c	USB Host	Power	GND	16
17	CAN_TX	CAN	UART-A	UART0_TXD#	18
19	CAN_RX			UART0_RXD#	20
21	47 kΩ PU	UART-E		47 kΩ PU	22
23	n/c			n/c	24
25	UART3_TXD	UART-D	Touch	Touch_XP	26
27	UART3_RXD			Touch_XM	28
29	UART2_TXD	UART-C		Touch_YP	30
31	UART2_RXD			Touch_YM	32
33	UART1_TXD	UART-B	A/D	ANA_IN1	34
35	UART1_RXD			ANA_IN2	36
37	n/c	A/D		n/c	38
39	+3V3	Power		GND	40
41	LCD_D22	LCD		LCD_D23	42
43	LCD_D20			LCD_D21	44
45	LCD_D18			LCD_D19	46
47	LCD_D16			LCD_D17	48
49	LCD_D14			LCD_D15	50
51	LCD_D12			LCD_D13	52
53	LCD_D10			LCD_D11	54
55	LCD_D8			LCD_D9	56
57	LCD_D6			LCD_D7	58
59	LCD_D4			LCD_D5	60
61	LCD_D2			LCD_D3	62
63	LCD_D0			LCD_D1	64
65	+3V3	Power		GND	66

67	n/c	**LCD**		LCD_CLKI	**68**
69	LCD_DISP			LCD_DCK	**70**
71	LCD_HSYN			LCD_DON	**72**
73	LCD_VSYN			LCD_VCPWC	**74**
75	VOU_DEST			LCD_VEPWC	**76**
77	VOU_RST#	**VIO0, VOU**		VIO_D7	**78**
79	n/c			VIO_D6	**80**
81	VIO_CKO			VIO_D5	**82**
83	VIO_CLK			VIO_D4	**84**
85	VIO_HD			VIO_D3	**86**
87	VIO_VD			VIO_D2	**88**
89	VIO_SRC			VIO_D1	**90**
91	VIO_RST#			VIO_D0	**92**
93	+3V3	**Power**		GND	**94**
95	SDC_D0	**SDC**	**SDIO**	SDI1_D0	**96**
97	SDC_D1			SDIO_D1	**98**
99	SDC_D2			SDIO_D2	**100**
101	SDC_D3			SDIO_D3	**102**
103	SDC_CMD			SDIO_CMD	**104**
105	SDC_CLK			SDIO_CLK	**106**
107	SDC_CD#			SDIO_CD#	**108**
109	SDC_WP			SDIO_WP	**110**
111	SPI_SS#	**SPI**		SPI_MISO	**112**
113	SPI_SCK			SPI_MOSI	**114**
115	SCL	**I2C**	**Audio**	AUDIO_BCK	**116**
117	SDA			AUDIO_LRC	**118**
119	n/c	**SPDIF**		AUDIO_DATI	**120**
121	GND			AUDIO_DATO	**122**
123	GND	**Power**		AUDIO_MCLK	**124**
125	GPIO_8	**GPIO**		GPIO_9	**126**
127	GPIO_6			GPIO_7	**128**
129	GPIO_4			GPIO_5	**130**
131	GPIO_2			GPIO_3	**132**
133	PWR_ON#			GPIO_1	**134**
135	3V3_ON	**PWR Control**	**Power**	GND	**136**
137	A22	**Address A[23:0]**		A23	**138**
139	A20			A21	**140**
141	A18			A19	**142**

143	A16		A17	**144**
145	A14		A15	**146**
147	A12		A13	**148**
149	A10		A11	**150**
151	A8		A9	**152**
153	A6		A7	**154**
155	A4		A5	**156**
157	A2		A3	**158**
159	GND		A1	**160**
161	+3V3	**Power**	GND	**162**
163	D14	**Data D[15:0]**	D15	**164**
165	D12		D13	**166**
167	D10		D11	**168**
169	D8		D9	**170**
171	D6		D7	**172**
173	D4		D5	**174**
175	D2		D3	**176**
177	D0		D1	**178**
179	BUS-CLK	**Bus Control**	n/c	**180**
181	BS#		10 kΩ PU	**182**
183	RD#		IRQ_GIO8	**184**
185	WE#		IRQ_GIO9	**186**
187	WE#		IRQ_GIO7	**188**
189	WE#		RESO#	**190**
191	RD#		RESI#	**192**
193	WE#		CS1#	**194**
195	WAIT#		CS2#	**196**
197	CS1#		n/c	**198**
199	BAT	**Power**	GND	**200**

6.2 J2, Debug Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	n/c	**2**	TCK
3	GND	**4**	GND
5	+1V8	**6**	TRST#
7	+3V3	**8**	+3V3
9	n/c	**10**	TDO
11	CFG_SCL	**12**	JTAG_DE#
13	CFG_SDA	**14**	TMS
15	CFG_WP	**16**	TDI
17	GND	**18**	JTAG_SEL
19	JTAG_RESI#	**20**	JTAG_RESI#

6.3 J3, Video Output

Type 30-pin connector, Hirose DF12(3.0)-30DS-0.5V (Receptacle)

Pin	Signal	Pin	Signal
1	GND	**2**	n/c
3	NTSC_D7	**4**	n/c
5	NTSC_D6	**6**	n/c
7	NTSC_D5	**8**	n/c
9	NTSC_D4	**10**	n/c
11	NTSC_D3	**12**	n/c
13	NTSC_D2	**14**	n/c
15	NTSC_D1	**16**	n/c
17	NTSC_D0	**18**	n/c
19	GND	**20**	GND
21	27MHZ_IN	**22**	n/c
23	NTSC_CLKO	**24**	n/c
25	n/c	**26**	n/c
27	n/c	**28**	n/c
29	GND	**30**	n/c

7 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	input
O	totem pole output
OD	open drain output
I/O	bidirectional

PU xK	pull-up resistor, x KΩ
PD xK	pull-down resistor, x KΩ
SR xR	series resistor x Ω
IPD	processor internal pull-down resistor, typ. 50 KΩ

7.1 J1, SODIMM Connector

Name	GPIO	Direction	Termination	Level [V]	Description
SPEED_LED#		OD	-	3.3	Speed indicator, 0 = 100Mb
ETH_TDP		AO	-	-	Ethernet TX pos.
ETH_TDM		AO	-	-	Ethernet TX neg.
ETH_RDP		AI	-	-	Ethernet RX pos.
ETH_RDN		AI	-	-	Ethernet RX neg.
LINK_LED#		OD	-	3.3	Traffic indicator
USBH_PEN#	GPIO_007	O	PU 47K	3.3	Power enable signal for VBUS switch
USBH_OC#	GPIO_008	I	PU 47K	3.3	Overcurrent signal from VBUS switch
USBH_DP		I/O	IPD 15K	-	USB data pos.
USBH_DM		I/O	IPD 15K	-	USB data neg.
USBF_VBUS		I	PD 15.6 K	5	VBUS detection
USBF_DP		I/O	-	-	USB data pos.
USBF_DM		I/O	-	-	USB data neg.
UART0_TXD#		O	-	RS232	UART transmit data
UART0_RXD#		I	-	RS232	UART receive data
UART1_TXD		O	PU 47K	3.3	UART transmit data
UART1_RXD		I	SR 1k	3.3	UART receive data
UART2_TXD		O	PU 47K	3.3	UART transmit data
UART2_RXD		I	SR 1k	3.3	UART receive data
UART3_TXD		O	PU 47K	3.3	UART transmit data
UART3_RXD		I	SR 1k	3.3	UART receive data
CAN_TX		O		3.3	CAN transmit data
CAN_RX		I	PU 10K	3.3	CAN receive data
TOUCH_XP		A I/O	-	3.3	X pos terminal
TOUCH_XM		A I/O	-	3.3	X neg terminal
TOUCH_YP		A I/O	-	3.3	Y pos terminal
TOUCH_YM		A I/O	-	3.3	Y neg terminal
ANA_IN1		AI	-	3.3	Analog input
ANA_IN2		AI	-	3.3	Analog input
LCD_DON	GPIO_003	O	IPD	3.3	LCD display enable signal

Name	GPIO	Direction	Termination	Level [V]	Description
LCD_DCK		O		3.3	LCD data clock
LCD_LCLK		I		3.3	External clock input for LCD
LCD_DISP		O		3.3	LCD data enable signal
LCD_VSYNC		O		3.3	LCD frame sync signal
LCD_HSYNC		O		3.3	LCD line sync signal
LCD_D[23:0]		O		3.3	LCD colour data
LCD_VEPWC	GPIO_009	O	IPD	3.3	Optional LCD power control
LCD_VCPWC	GPIO_010	O	IPD	3.3	Optional LCD power control
VOU_DEST	GPIO_026	O	IPD	3.3	optional video output switch
VOU_RST#	GPIO_028	O	IPD	3.3	optional video output reset
VIO_CLK		O		3.3	Camera clock output
VIO_CKO		I		3.3	Camera clock input
VIO_HD		I		3.3	Video hsync input
VIO_VD		I		3.3	Video vsync input
VIO_D[7:0]		I		3.3	Camera input data
VIO_SRC	GPIO_017	O	IPD	3.3	Optional selection of video source
VIO_RST#	GPIO_006	O	IPD	3.3	Optional reset signal for external video decoder
SDC_CMD		I/O	IPD	3.3	SDC CMD signal
SDC_CLK		O	IPD	3.3	SDC clock output
SDC_D[3:0]		I/O	IPD	3.3	SDC data
SDC_CD#	GPIO_014	I	PU 10K	3.3	SDC card detect input
SDC_WP	GPIO_013	I	PU 10K	3.3	SDC write protect input
SDIO_CMD		I/O	IPD	3.3	SDIO CMD signal
SDIO_CLK		O	IPD	3.3	SDIO clock output
SDIO_D[3:0]		I/O	IPD	3.3	SDIO data
SDIO_CD#	GPIO_012	I	PU 10K	3.3	SDIO card detect input
SDIO_WP	GPIO_011	I	PU 10K	3.3	SDIO write protect input
SPI_SS#		I/O		3.3	SPI Slave select
SPI_SCK		I/O		3.3	SPI Clock
SPI_MISO		I		3.3	Input data from slave
SPI_MOSI		O		3.3	Output data to slave
SCL		O	PU 2K2	3.3	I^2C clock output
SDA		I/O	PU 2K2	3.3	I^2C data signal
AUDIO_BCK		I/O		3.3	PCM bit clock
AUDIO_LRC		I		3.3	PCM L/R signal
AUDIO_DATI		I	SR 1K	3.3	PCM input data
AUDIO_DATO		O		3.3	PCM output data
AUDIO_MCLK		O		3.3	Optional PCM oversampling clock
PWR_ON#		I	SR 1K	3.3	Optional power on input
GPIO_1	PMIC GPIO5	I	SR 1K, PD4K7	3.3	Digital I/O
GPIO_2	GPIO_029	I/O	SR 1K	3.3	Digital I/O
GPIO_3	GPIO_015	I/O	SR 1K	3.3	Digital I/O
GPIO_4	GPIO_120	I/O	SR 1K	3.3	Digital I/O, PWM output
GPIO_5	GPIO_121	I/O	SR 1K	3.3	Digital I/O, PWM output
GPIO_6	GPIO_031	I/O	SR 1K	3.3	Digital I/O
GPIO_7	GPIO_030	I/O	SR 1K	3.3	Digital I/O
GPIO_8	GPIO_104	I/O	SR 1K	3.3	Digital I/O
GPIO_9	GPIO_102	I/O	SR 1K	3.3	Digital I/O
3V3_ON		O		3.3	Control signal for 3V3 supply of external parts

Name	GPIO	Direction	Termination	Level [V]	Description
A[23:1]		O		3.3	Processor address bus
A0		-		-	GND, bus interface does not support A0
D[15:0]		I/O	SR 82R	3.3	Processor data bus
CKIO		O	SR 82R	3.3	66 MHz bus clock
BS#		O	PU 47K	3.3	Bus start output
WAIT#		I	PU 1K	3.3	Wait input
CS1#		O	PU 47K	3.3	Chip select output
CS2#		O	PU 47K	3.3	Chip select output
RD#		O	PU 47K, SR 82R	3.3	Read signal
WE#		O	PU 47K, SR 82R	3.3	Write access on even address
NMI	GPIO_114	I	PU 10K, SR 1K	3.3	Interrupt input
IRQ-A	GPIO_143	I	PU 10K	3.3	Interrupt input
IRQ-B	GPIO_144	I	PU 10K	3.3	Interrupt input
RESI#		I	PU 47K	3.3	Reset input
RESO#		O	-	3.3	Reset output
BAT		-	-	1.9 … 3.3	Backup battery input for RTC
+3V3		-	-	-	+ 3.3V supply
GND		-	-	-	Ground

7.2 J2, Debug Connector

Name	Direction	Termination	Level [V]	Description
JTAG Interface				
TCK	I		1.8	JTAG clock
TMS	I		1.8	JTAG mode select
TRST#	I		1.8	JTAG test reset
TDI	I		1.8	JTAG data in
TDO	O		1.8	JTAG data out
JTAG_RESET#	I	PU 1K	1.8	JTAG reset in
JTAG_DE#	I	PU 10K	1.8	JTAG TDOEN
JTAG_SEL	I	PD 1K	1.8	JTAG_SEL
Others				
CFG_SCL	O	PU 4K7	3.3	used for production
CFG_SDA	I/O	PU 4K7	3.3	used for production
CFG_WP	I	PU 4K7	3.3	used for production
+1V8	-	-	-	+ 1.8V supply
+3V3	-	-	-	+ 3.3V supply
GND	-	-	-	Ground

7.3 J3, Video Output Connector

Name	Direction	Termination	Level [V]	Description
Video Out Interface				
NTSC_D0	O	-	3.3	YUV data
NTSC_D1	O	-	3.3	YUV data
NTSC_D2	O	-	3.3	YUV data
NTSC_D3	O	-	3.3	YUV data
NTSC_D4	O	-	3.3	YUV data
NTSC_D5	O	-	3.3	YUV data
NTSC_D6	O	-	3.3	YUV data
NTSC_D7	O	-	3.3	YUV data
NTSC_CLKO	O	-	3.3	Video clock output
27MHZ_IN	I	-	3.3	27 MHz clock input
Others				
GND	-	-	-	Ground

8 Technical Characteristics

8.1 Electrical Specifications

Supply voltage	3.3 V, +/-5%
Current consumption	0.35 A max.

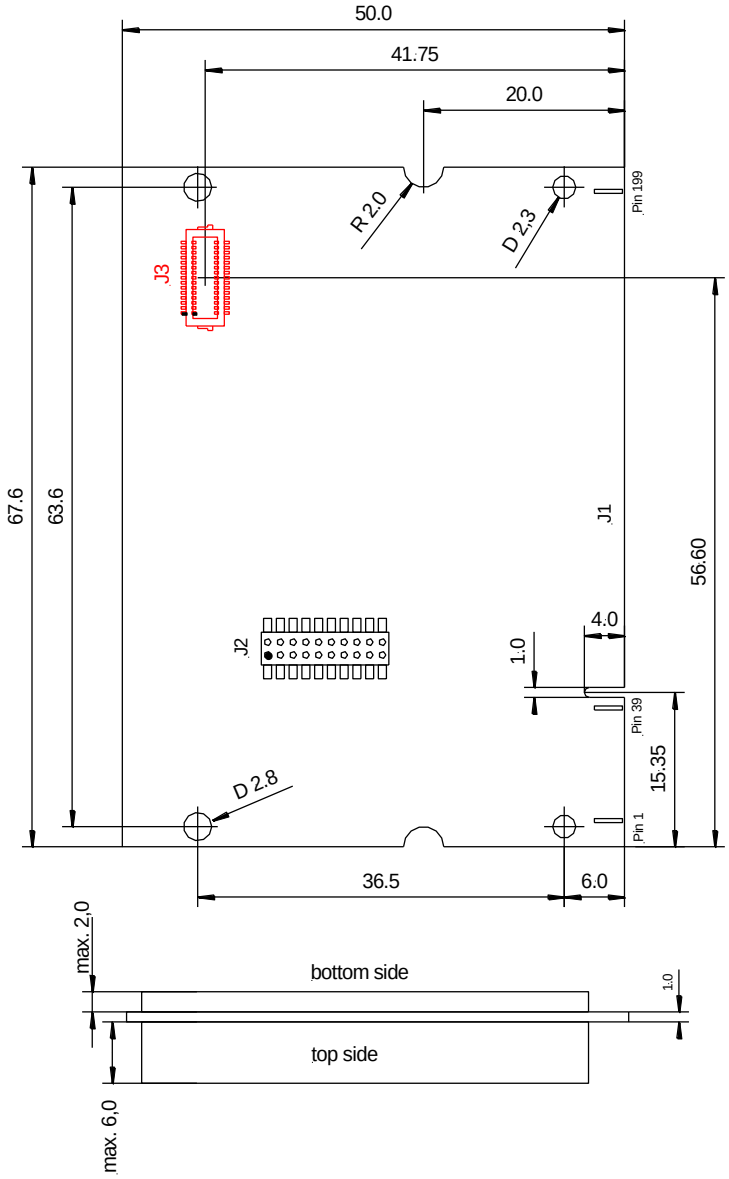
8.2 Environmental Specifications

Operating temperature **Storage temperature**	-10°C ... +70°C -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

8.3 Mechanical Specifications

Weight	approx. 15 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 50.0 mm x 10.0 mm

8.4 Dimensional Drawing



Connector J3 is located on the bottom side of the DIMM module.

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