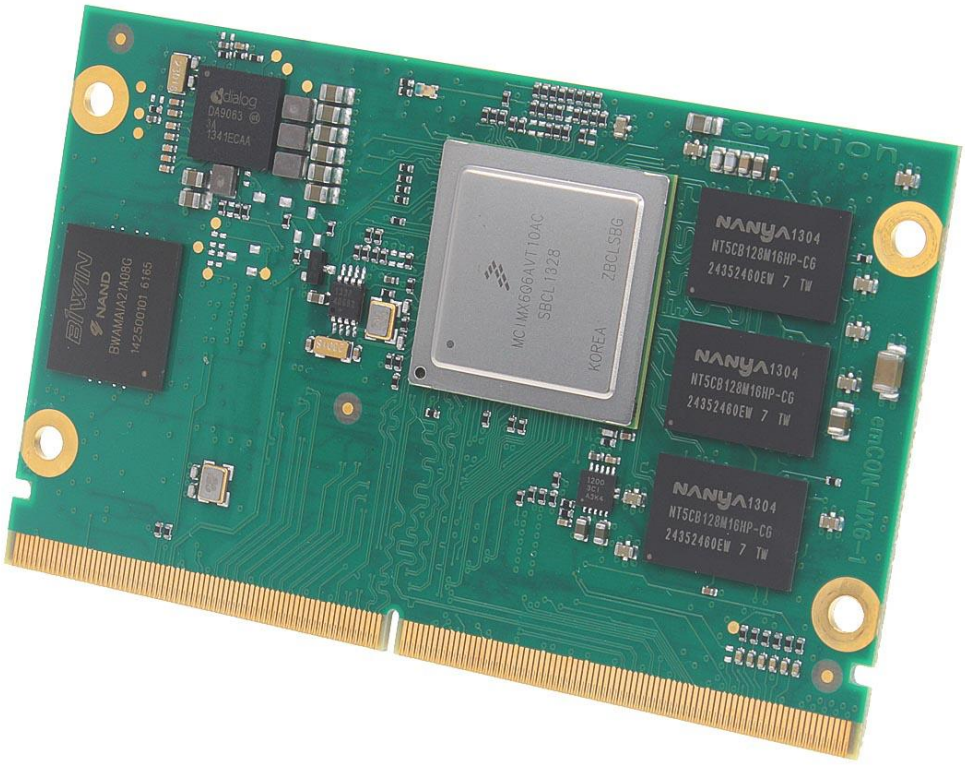
emCON-MX6

Hardware Manual

Rev2 / 13.10.2017



emtrion GmbH

Revision: **2 / 13.10.2017**

Rev	Date/Signature	Changes
1	17.05.2015/Sr	First revision
2	13.10.2017/We	Typos corrected Connector J1 in chapter 6.1 (SPI-2) corrected

Contents

1 Introduction

The emCON-MX6 processor module is a CPU board of emtrion's emCON-family based on the i.MX6 processor from Freescale. The i.MX6 includes up to 4 ARM Cortex A9 cores.

emCON-MX6x processor modules with i.MX6 Quad core, dual core, dual light core or single core are available. Please contact emtrion GmbH for further information.

The processor cores run up to 1 GHz and include a variety of functions required for multimedia or industrial applications. These include a MPEG4 and H.264 encoder, a 3D graphics accelerator, LCD controller, two LVDS interfaces, HDMI interface, two camera interfaces and a sound input/output module.

The module can be ordered with different sizes of NAND-Flash and RAM and different amounts of ARM Cortex A9 cores. The CPU has an internal Ethernet MAC, two CAN controllers and two USB controllers, which are used as USB Host and USB Device.

All interfaces are accessible through a 315 pin MXM type III edge connector. The pin assignment is defined in emtrion's emCON standard, which ensures a pin-to-pin compatibility with all emCON CPU modules.

In the following table the features and interfaces of the emCON-MX6 processor module are described.

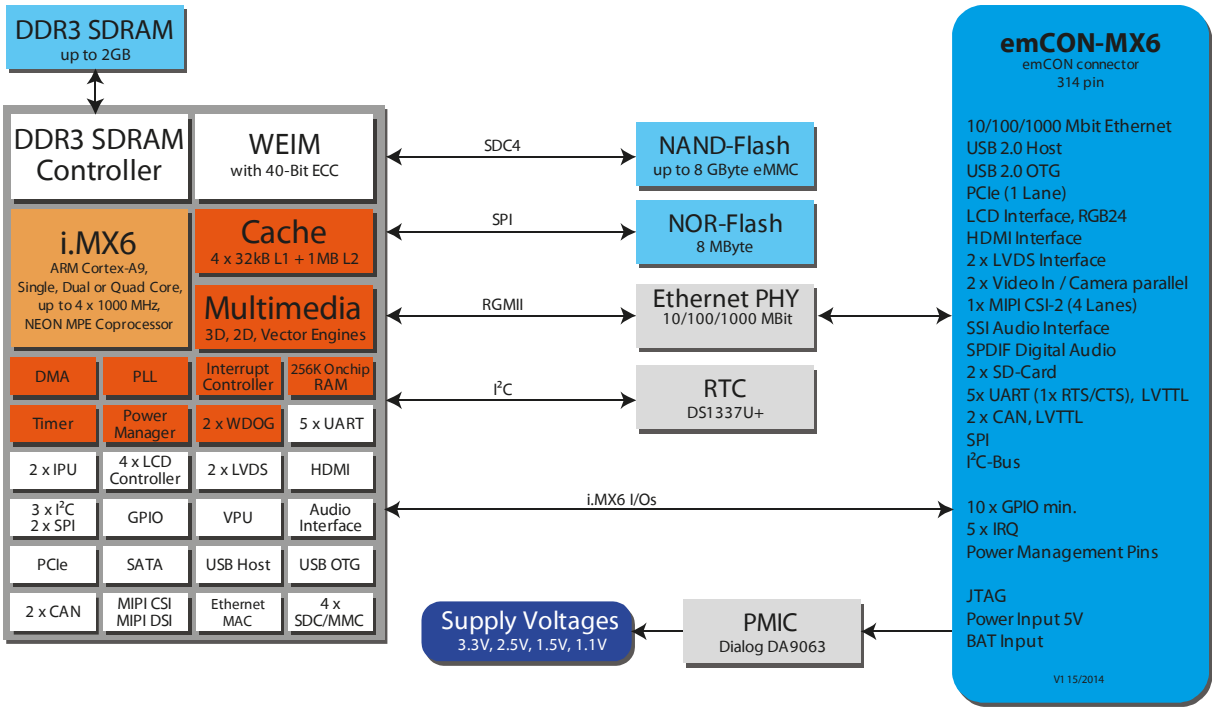
emCON-MX6
1GB/2GB SDRAM
up to 32GB eMMC NAND Flash
1x 10/100/1000 Mbit Ethernet
1x USB Host
1x USB Device
1x SATA
1x PCIe (1 lane)
1x LCD Interface 16/18/24bit max. 1080p (1920x1080)
2x LVDS 24bit max. UXGA (1600x1200) in split mode
1x HDMI 24bit max. 1080p(1920x1080)
2x Video IN 8bit
1x MIPI CSI-2 (4 lanes)
1x SSI Audio
1x SPDIF
2x CAN (LVTTL)
5x UART (LVTTL)
2x SD Card
1x SPI
2x I2C (one internal, one external)
8x GPIO, 3x PWM
RTC, battery buffered
JTAG

Please contact emtrion GmbH for the available processor, NAND Flash and SDRAM configurations.

The module is available in the standard temperature range 0°C to 70°C and in the extended temperature range -40°C to 85°C.

2 Block Diagram

The following figure shows the block diagram of the emCON-MX6.



3 Handling Precautions

Please read the following notes prior to installing the processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The module does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatically discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The emCON-MX6 processor module uses the i.MX processor i.MX6x from Freescale [1]. It includes up to 4 ARM Cortex A9 cores and runs up to 1 GHz.

In addition to the CPU core with MMU, FPU and Caches, this processor provides a lot of features such as:

- NAND Flash controller
- DDR3 SDRAM controller
- Ethernet MAC 10/100Mbit with IEEE1588 support
- USB 2.0 Host with high-speed mode
- USB 2.0 OTG with high-speed mode
- 2 SD Card host controllers
- Two Image Processing Units which includes
    - Two Video input modules with camera capturing module
    - LCD Controller for TFT displays up to 1080p (1920x1080) @60Hz and 16/18/24 bpp
    - 24bit LVDS display port up to WXGA (1366x768) @60Hz and 16/18/24 bpp
    - 24bit HDMI port up to 1080p (1920x1080) @60Hz and 16/18/24 bpp
    - 2D and 3D graphic hardware accelerator
    - NEON SIMD media accelerator
- 4 wire Touch controller
- Two CAN controllers
- 5 UARTs with 2x 32 byte FIFO
- I2C bus interfaces
- SPI interfaces
- IrDA interfaces
- Watchdog timer
- Real time clock
- Sound interface with I2S format
- Sound interface SPDIF in and out
- SATA controller

- Interrupt controller
- 32-bit timer
- JTAG debug interface

Further details of the processor can be found in the i.MX6x Reference Manual [1].

4.1.1 Processor Clocks

The 24MHz main clock is generated by a quartz crystal. Eight internal PLLs multiply the 24MHz main clock to the internal clocks. All clocks within the processor are derived from theses frequencies, via various software configurable dividers.

The core clock (PLL1) can be up to 1,2 GHz. For power management, the core clock can be varied.

It must be considered that the core voltage should be adapted if the core frequency is varied.

More information about the i.MX6 clock system is described in the CCM chapter of the i.MX6 Reference Manual [1].

The RTC_XTALI clock input of the CPU is supplied by a 32,768 kHz clock from the RTC chip. That RTC chip is connected to a 32,768 kHz quartz crystal. This clock swings even when the main supply is switched off and an auxiliary voltage (2,3V – 3,3V) is connected at the BAT pin of the emCON connector.

4.1.2 Boot Mode

The emCON-MX6 Uboot can be booted either from the onboard eMMC, the SD-Card interface or external via the USB Device interface. The boot mode is configured via three boot mode signals which are available at the emCON connector. A dip switch on the carrier board is used to configure the boot mode.

BOOT_MODE_1	BOOT_MODE_2	BOOT_MODE_3	Boot source
LOW	HIGH	LOW	eMMC
LOW	HIGH	HIGH	SD-Card 1
HIGH	LOW	X	USB (Serial)
LOW	LOW	X	Boot from Fuses
HIGH	HIGH	X	Reserved

4.2 NAND-Flash

To store the operating system and application data, a eMMC NAND Flash is provided on the emCON-MX6 module. It is connected to the uSDHC3 controller of the i.MX6.

The NAND Flash size can be between 4GB and 32GB depending on the ordering code.

Please contact emtrion GmbH for your required NAND Flash size.

The onboard NAND Flash controller can be reset either by the global reset signal RESO# or by uSDHC3 reset function or by the GPIO7-8 if the i.MX6 pin SD3_RST is configured as a GPIO output. A low at the signal SD3_RST resets the NAND Flash controller.

4.3 DDR3 SDRAM

DDR3 SDRAM is available as main memory. The RAM memory has a 64bit width interface and can be clocked up to 528MHz. In a standard SW configuration the i.MX6 PLL2 is responsible for the RAM clock.

The SDRAM size can be between 512MB and 2GB, depending on the ordering code. The following table shows the address range for the different RAM sizes.

RAM size	Start address	End address
512MB	0x10000000	0x2FFFFFFF
1GB	0x10000000	0x4FFFFFFF
2GB	0x10000000	0x8FFFFFFF

Please contact emtrion GmbH for your required RAM size.

4.4 Ethernet

The Ethernet interface is realized with the processor internal Media Access Controller (MAC) and an external Physical Layer Interface (PHY) KSZ9031RNX from Micrel. The RGMII interface is used for communication between the MAC and the PHY.

The Ethernet interface supports the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. HP Auto-MDIX is also supported.

The registers of the Ethernet PHY can be configured via the Media Independent Interface (MII).

The Ethernet signal lines (GBE1_MDI[0:3]_P, GBE1_MDI[0:3]_N) as well as two status signals that serve to indicate the link status and the transfer speed are connected to the emCON connector. An appropriate 1:1 transformer with a 100nF capacitor to GND at each center tap pin must be added externally. The center tap pin shall not be supplied with 3.3V!

The emCON pin GBE1_LED_10_100# and GBE1_LED_1000# are both connected to the LED2 pin of the Ethernet PHY and indicate if a link is established. (“0” = link). Therefore the link speed has to be determined by software.

The emCON pin GBE1_LED_TRAFFIC# is connected to the LED1 pin of the Ethernet PHY indicates if the data is transferred (“blinking” = traffic).

The RGMII 125MHz Ethernet clock is generated by the PLL of the Ethernet PHY and is routed to the processors internal MAC.

The Ethernet Phy can be reset either by the global reset signal RESO# or by the GPIO5-20 if the i.MX6 pin IPU1_CSI0_DATA_EN is configured as a GPIO output. A low at this pin resets the Ethernet PHY.

4.5 USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the internal host controller of the i.MX6x. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed (1,5Mbps), full-speed (12 Mbps) and high-speed (480Mbps).

To switch the bus power the control line USBH_PEN# is connected to the emCON connector. A logical "0" at the processor GPIO3-31 switches the power on; a logical "1" turns the power off. The signal USBH_OC# reports an overcurrent at the GPIO3-30 ("0" = overcurrent).

The data lines and the two control lines are available at the emCON connector. A USB power switch must be added externally. The data lines are internally terminated with 15-KΩ pulldown resistors.

The USBH_VBUS signal on the emCON connector is only an input to detect the VBUS voltage on the baseboard.

4.6 USB OTG

The USB OTG port can operate in Host or Device mode. The signal USBOTG_ID is used to determine the mode of the connected device.

The interface is realized by the internal device controller of the i.MX6x. The interface is USB 2.0 compliant, supporting data transfers at low-speed (1,5Mbps), full-speed (12 Mbps) and high-speed (480Mbps).

To switch the bus power in USB Host mode the control line USBOTG_PEN# is connected to the emCON connector. A logical "0" at the processor GPIO1-8 switches the power on; a logical "1" turns the power off. The signal USBH_OC# reports an overcurrent at the GPIO1-7 ("0" = overcurrent).

The USBOTG_VBUS signal on the emCON connector is only an input to detect the VBUS voltage on the baseboard.

4.7 Graphic Displays

The emCON-MX6 has four display ports. The first is a 24bit TFT display port, the second is a 24bit HDMI display port and additional are two 24bit LVDS display ports available.

The i.MX6 includes two Image Processing Units (IPU). One IPU can display up to two different images. Maximum four independent images can be displayed on the four available display ports. This can be configured via software.

More information about the i.MX6 Multimedia system is described in the Multimedia and IPU chapter of the i.MX6 Reference Manual [1].

4.7.1 TFT

The LCD controller of the i.MX6 can drive TFT displays with resolutions up to 1080p (1920x1080) at 16/18/24bpp. The pixel clock for the display data can be generated by an internal PLL.

The LCD interface can be used by IPU1 (IPU1_DI0) and IPU2 (IPU2_DI0).

All data and control lines are available at the emCON connector. The following table describes the function of the data and control lines.

Signal	Description
LCD_D[23:0]	24 color data; can also be used in 18 or 16 bit mode
LCD_VSYNC	Vertical synchronization signal
LCD_HSYNC	horizontal synchronization signal
LCD_DE	Data enable signal, if active colour data are valid
LCD_PIXCLK	Display clock
LCD_PANEL_EN	Display power enable signal, GPIO7-9
LCD_BL_EN	Backlight power enable signal, GPIO6-8
LCD_BL_CTRL	PWM signal to control the backlight, GPIO2-9, PWMO3

The following table shows the RGB colour mapping on the LCD_D[23:0] pins of the emCON connector.

LCD_D[17:0]	RGB565 (16bit)	RGB666 (18bit)	RGB888 (24bit)
LCD_D0	B0	B0	B0
LCD_D1	B1	B1	B1
LCD_D2	B2	B2	B2
LCD_D3	B3	B3	B3
LCD_D4	B4	B4	B4
LCD_D5	G0	B5	B5
LCD_D6	G1	G0	B6
LCD_D7	G2	G1	B7
LCD_D8	G3	G2	G0
LCD_D9	G4	G3	G1
LCD_D10	G5	G4	G2
LCD_D11	R0	G5	G3
LCD_D12	R1	R0	G4
LCD_D13	R2	R1	G5

LCD_D14	R3	R2	G6
LCD_D15	R4	R3	G7
LCD_D16	-	R4	R0
LCD_D17	-	R5	R1
LCD_D18	-	-	R2
LCD_D19	-	-	R3
LCD_D20	-	-	R4
LCD_D21	-	-	R5
LCD_D22	-	-	R6
LCD_D23	-	-	R7

4.7.2 LVDS

The LCD controller of the i.MX6 can drive two LVDS interfaces. The pixel clock for the display data can be generated by an internal PLL.

For single-channel LVDS output the pixel clock is limited to 85 MHz per LVDS port. This results in a maximum resolution of WXGA (1366x768 @ 60HZ with 35% blanking), for example. If a higher resolution is needed, the split mode has to be used. In this case one LVDS port outputs ODD data and the other port EVEN data. The pixel clock is limited to 170 MHz (e.g. UXGA 1600x1200 @ 60 Hz with 35% blanking). To use the split mode, a display supporting the dual channel LVDS mode in order to receive odd and even pixel data is needed!

The LVDS interfaces can be used by both IPU1 display units (IPU1_DI0 and IPU1_DI1) and both IPU2 display units (IPU2_DI0 and IPU2_DI1).

The following table describes the signals of LVDS port 1:

Signal	Description
LVDS1_CLK_P/N	Differential LVDS clock
LVDS1_D[3:0]_P/N	Four differential LVDS data signal pairs
LVDS1_PANEL_EN	Display power enable signal, GPIO7-10
LVDS1_BL_EN	Backlight power enable signal, GPIO6-9
LVDS1_BL_CTRL	PWM signal to control the backlight, GPIO1-9, PWMO1

The following table describes the signals of LVDS port 2:

Signal	Description
LVDS2_CLK_P/N	Differential LVDS clock
LVDS2_D[3:0]_P/N	Four differential LVDS data signal pairs

In the 24 bit mode the colour mapping can be different depending of the used display. The colour mapping can be set by a register bit. The following table shows the 18/24bit colour mapping in the SPWG/PSWG/VESA mode.

Signal	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_TX0	G0	R5	R4	R3	R2	R1	R0
LVDS_TX1	B1	B0	G5	G4	G3	G2	G1
LVDS_TX2	DE	VS	HS	B5	B4	B3	B2
LVDS_TX3 (only for 24bit)	CTL	B7	B6	G7	G6	R7	R6

The following table shows the 24bit colour mapping in the JEIDA mode.

Signal	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_TX0	G2	R7	R6	R5	R4	R3	R2
LVDS_TX1	B3	B2	G7	G6	G5	G4	G3
LVDS_TX2	DE	VS	HS	B7	B6	B5	B4
LVDS_TX3	CTL	B1	B0	G1	G0	R1	R0

4.7.3 HDMI

The LCD controller of the i.MX6 can drive HDMI with a resolution up to 1080p at 60Hz. The pixel clock for the display data is generated by an internal PLL.

The HDMI interface can be used by both IPU1 display units (IPU1_DI0 and IPU1_DI1) and both IPU2 display units (IPU2_DI0 and IPU2_DI1).

Audio data can be transmitted, too.

The HDMI I^2C interface can be used for communication with the connected display. The bus has only the i.MX6 internal pullup resistors, which are not suitable for fast I^2C communications. To use the I^2C bus pullups in the range of 2.2kΩ - 4.7kΩ have to be placed on the baseboard.

The following table describes the HDMI signals:

Signals	Description
HDMI_D[2:0]_P/N	Three differential HDMI data signal pairs
HDMI_CLK_P/N	Differential HDMI clock
HDMI_SCL	HDMI I^2C clock signal
HDMI_SDA	HDMI I^2C data signal
HDMI_CEC	Consumer Electronics Control (CEC) signal
HDMI_HPD	Hot plug detecting signal

The signals HDMI_SDA, HDMI_SCL and HDMI_HPD must have 3.3V level and cannot be connect directly to the HDMI connector which has a 5V signal level. The level translation can be done with a HDMI level shifter on the baseboard.

4.8 Video Input

The emCON-MX6 has two video input units (CSI0 and CSI1) which can be used with different video sources, such as video codecs or CMOS camera modules.

The CSI0 and CSI1 interfaces at the emCON-MX6 are realised with an 8-bit data-bus available at the emCON connector and supports various input formats.

The CSI0 interface can be used by the IPU1 and is named CPI1 at the emCON connector.

The following table describes the CPI1 signals.

Signals	Description
CPI1_D[7:0]	Video input data
CPI1_PIXCLK	Video input clock
CPI1_HSYNC	Video input horizontal synchronization
CPI1_VSYNC	Video input vertical synchronization

The CSI1 interface of the i.MX6 can be used by the IPU2. Because the emCON connector has only one parallel camera interface the second interface is available at the RFU (reserved for future use) pins. This pins are reserved for CPU specific interfaces which are normally not available at other CPUs.

The following table describes the CPI2 signals at the RFU pins.

Signals	Description
CPI2_D[7:0]	Video input data
CPI2_PIXCLK	Video input clock
CPI2_HSYNC	Video input horizontal synchronization
CPI2_VSYNC	Video input vertical synchronization

CSI0_DATA_EN and CSI1_DATA_EN are used for other functions. Do not mux this pins to the CSI interfaces.

4.9 MIPI CSI-2

The MIPI CSI-2 interface is serial interface with differential data pairs to transport camera data with higher bandwidth than the parallel interface. The i.MX6 comes with 4 data lanes which supports up to 1000Mbps per lane and one clock pair.

The following table describes the MIPI CSI-2 signals available at the emCON interface.

4.10 Audio Interfaces

4.10.1 I2S Audio

The integrated audio module (AUD3) of the i.MX6 can be used to send and receive audio data from external audio codecs.

The sampling rate is configurable by software, but is always the same for playback and recording.

The interface is connected to the emCON connector, which allows the selection of an external audio codec.

4.10.2 Audio SPDIF

The emCON-MX6 also supports to output audio data in the SPDIF format. The SPDIF_OUT signal at the emCON connector has LVTTL level and will need to be configured external according to the SPDIF specification.

Because of the pin multiplexing the SPDIF_IN pin of the emCON connector has to be left floating.

4.11 SD-Card Interface

The i.MX6x includes four SD Card interfaces to drive memory- or I/O cards. Two of them (uSDHC1 and uSDHC2) are used for the two 4bit SD Card interfaces of the emCON connector. uSDHC1 is used for the interface SDC1. uSDHC2 is used for the interface SDC2.

The card detect and write protect signals can be controlled either by the two SD card controller uSDHC1 and uSDHC2 or by the GPIO ports of the i.MX6x:

Signal	Description	GPIO
SDC1_CD#	Low-active card detection signal	GPIO1_1
SDC1_WP	high-active write protection signal	GPIO4_20
SDC2_CD#	Low-active card detection signal	GPIO1_4
SDC2_WP	high-active write protection signal	GPIO1_2

4.12 Serial Ports

The emCON-MX6 has five serial ports. All serial ports are integrated in the processor i.MX6x and available as LVTTL level. To use the interfaces as RS232 or RS485 external transceivers are necessary.

An overview of the UART interfaces is shown in the following table:

i.MX6 interface	emCON name	Handshake Signals
UART1	UART_A	-
UART2	UART_B	RTS, CTS
UART3	UART_C	-
UART4	UART_D	-
UART5	UART_E	-

UART1 is used as standard debug and communication interface (TERMINAL).

4.12.1 IrDA

Each processor UART port can also be used as low speed (115200bps) Infrared port (IrDA). The UART RXD input signal is also the IrDA RXD input signal. The UART TXD output signal is the IrDA TXD output signal.

4.13 I²C- Bus

On the emCON-MX6 are two I²C bus interfaces available.

The first I²C interface (I2C1) is only routed on the emCON-MX6 and all onboard I²C devices on the module are connected to that interface. The interface works with a transmission speed up to 100 kb/s. The interface operates as a master.

Two devices are connected to the I2C1 bus on emCON-MX6:

Slave	Device	Chip Address (7bit)
Real Time Clock	DS1337U+	0x68
PMIC	DA9063	0x58

The second I²C interface (I2C3) is routed to the emCON connector and can be used exclusive for baseboard functions. The maximum I²C speed is 400kb/s.

The external I²C interface can be used either in Master mode (default) or in Slave mode. In Slave mode the I²C address can be defined in i.MX6 register.

The bus connects to the emCON connector. The SCL and SDA lines are pulled up with 2,2kΩ resistors to 3,3V, so additional termination is not required.

4.14 SPI Interface

The SPI interface eCSPI2 of the i.MX6x processor is connected to the SPI1 interface of the emCON connector.

The SPI2 interface of the emCON connector is unused.

4.15 CAN

The i.MX6 includes two CAN controller, which are full implementations of the CAN protocol specification 2.0B, supporting both standard and extended message frames. The TX and RX signals are routed to the emCON connector. For each CAN interface a CAN transceiver must be realized on the base board.

The signal level is 3,3V. The maximum baud rate is 1Mbps.

4.16 SATA

The i.MX6x includes a SATA controller and a SATA phy. The SATA controller is compliant with the SATA specification 3.0 at 1,5Gb/s and 3,0Gb/s.

The SATA signals are routed to the emCON connector. The required AC coupling (12nF) at TX and RX signals is done on the emCON-MX6 module.

More details of the SATA controller can be found in the i.MX6x Reference Manual [1].

4.17 PCI Express

emtrion offers a special version of the CPU module which provides PCI Express Gen 2.0 functionality.

The i.MX6 processor includes the following PCI Express cores:

- PCI Express Dual Mode (DM) core
- PCI Express Root Complex (RC) core
- PCI Express Endpoint (EP) core

One PCI Express lane is supported.

The required AC coupling (220nF) at the TX and CLK pair is done on the emCON-MX6 module.

More details of the PCI Express controller can be found in the i.MX6x Reference Manual [1].

4.18 General Purpose I/Os

The emCON interface supports eight dedicated GPIOs which are directly connected to the CPU.

emCON Signal	i.MX6 Port	Direction
GPIO_1	GPIO2-0	In/Out
GPIO_2	GPIO2-1	In/Out
GPIO_3	GPIO2-2	In/Out
GPIO_4	GPIO2-3	In/Out
GPIO_5	GPIO2-4	In/Out
GPIO_6	GPIO2-5	In/Out
GPIO_7	GPIO2-6	In/Out
GPIO_8	GPIO2-7	In/Out

The signal level of each GPIO pin is 3,3V.

4.19 PWM

The i.MX6 includes four PWM modules. Three of them are available on the emCON connector:

emCON Signal	PWM Channel	Remark
LVDS1_BL_CTRL	PWM1	Backlight dimming
LCD_BL_CTRL	PWM3	Backlight dimming
PWM_FAN	PWM4	Fan control

The signal level of each PWM pin is 3,3V.

4.20 Status LED

A bicolour LED is connected to the port pins GPIO3-0 and GPIO3-1 of the i.MX6. If GPIO3-0 is high the green LED is lighting, if GPIO3-1 is high the red LED is lighting.

4.21 Interrupts

The processor i.MX6 has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor.

Generally each GPIO input can be configured as an interrupt input.

On the emCON-MX6 there are some GPIOs defined as interrupts. The interrupt sources are shown in the following table:

Signal	Source	i.MX6 GPIO Port	polarity	i.MX6 IRQ
IRQ_1	emCON connector	**GPIO6-7**	configurable	108
IRQ_2	emCON connector	**GPIO6-15**	configurable	108
IRQ_3	emCON connector	**GPIO6-16**	configurable	109
IRQ_TOUCH1#	emCON connector	**GPIO1-5**	configurable	98
IRQ_TOUCH2#	emCON connector	**GPIO6-31**	configurable	109
IRQ_RTC#	RTC (DS1337)	**GPIO2-11**	low active	100
PMIC_IRQ#	PMIC (DA9063)	**GPIO2-8**	low active	100
POWERFAIL#	emCON connector	**GPIO3-23**	high active	103

IRQ_A, IRQ_B and IRQ_C are general purpose interrupts from the emCON connector. The signal level of each interrupt is 3,3V.

IRQ_TOUCH1# and IRQ_TOUCH2# are interrupts from the emCON connector reserved for external touch controllers. The signal level of each interrupt is 3,3V.

The RTC interrupt can be asserted by the onboard RTC chip.

The PMIC interrupt can be asserted by the onboard Power Management chip.

The Power OFF interrupt is immediately asserted if the RESI# emCON pin is set to low. With this interrupt the SW can shut down itself until a hard reset is asserted 1s later.

4.22 Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the board voltages. If one voltage is out of tolerance a module reset is asserted. The reset time in that case is min 15ms.
- The active low signal RESI# and the signal JTAG_RESI# at the emCON connector, can assert a reset.
- A processor internal SW reset is available at a processor pin, if the pin function SYSTEM_RST is enabled. In this case the RESO# pin is asserted if a SW reset is asserted.

All resets are hardware resets of the whole board. All resets except the internal SW reset issue a processor cold reset. The internal SW reset issues a processor warm reset.

The duration of the reset signal is min. 15ms. For resetting external devices the reset signal is available as an output (RESO#) at the emCON connector.

4.23 Power Supply

The typical power consumption is between 0.8A-3A at +5V, +/- 5%, depending on the running software tasks, which must be supplied via the emCON connector. The onboard required voltages for the processor and the other parts are generated on board via a Power Management (PMIC) chip and the i.MX6 processor. The PMIC generates the input voltages for the i.MX6. The i.MX6 internal LDO's generate the power supply voltages for the i.MX6 cores and modules.

The voltages generated by the PMIC can be configured via the I^2C interface. The voltages generated by the i.MX6 can be configured via processor internal registers. During operation the voltages can be varied depending on the core frequencies and die temperature.

The 7-Bit I^2C-Address of the PMIC is 0x58:

More details about DVFS (Dynamic Voltage and Frequency Scaling) and power supply variation are described in the chapter 26 of the i.MX6 Reference Manual [1].

4.23.1 Signal Description

VCC_STANDBY & VCC_5V:

The 5v power supply is divided in two voltage areas. VCC_STANDBY is used powering up and to keep the PMIC and the most important voltages of the CPU alive during power down states. VCC_5V is the main supply and used to supply the board in the running state.

If power management is used the VCC_5V can be disabled in deep power down states. The disabling can be done with a mosfet circuit at the baseboard. To control the mosfet the signal SUSPEND# is available at the emCON interface. Example schematics are available.
VCC_STANDBY has to be kept on all the time.

If no power management is needed, VCC_STANDBY and VCC_5V can be both connected to 5V directly.

POWER_ON_BASE:

During some power down states the 3.3V areas of the CPU module will be switched off. In this case all the peripheral chips which are connected to 3.3V referenced signals have to be switched off, too. Otherwise the CPU will be back-powered via the I/O pins.

The signal POWER_ON_BASE can be used to control a DC/DC converter or a mosfet to switch the 3.3V on the baseboard on and off. A high signalize to switch on the 3.3V. Example schematics are available.

POWERFAIL#

The signal POWERFAIL# is an input to signalize a power fail condition. A low will trigger an interrupt e.g. to safe data.

ON_OFF# & WAKEUP:
The signals ON-OFF# and Wakeup are used to control the PMIC to getting up from power down states.

BAT:
The emCON BAT pin is the battery input pin for the RTC power supply. The typical power consumption of the RTC via the BAT pin is < 1µA.

4.23.2 Power Consumption
tbd

5 emCON Interface

All interface signals of the board are available at the emCON connector.

The emCON interface is a 314 pos MXM connector. These sockets are available from various manufacturers.

The pin assignment is emtrion specific and match for the most needs of interfaces for actual embedded designs. Depending on the features of the CPUs every emtrion CPU module will use a subset of the emCON connector. More details can be found in emtrion's emCON specification.

Usage details of the connector and its electrical and mechanical characteristics can be found further down in this document.

Notes:

The pin assignment of the emCON connector is ONLY compatible with devices of emtrion's emCON-family. Insertion into a socket with another pin assignment may damage the emCON-MX6 module and the carrier board.

Most of the pins are directly connected with the processor i.MX6x.

6 Pin Assignments

6.1 J1, emCON Connector

Type MXM, 314 pos
Possible carrierboard connector: Aces 91782-3140M-001

Notes:

The pin assignment of the emCON connector is ONLY compatible with devices of emtrion's emCON-family. Insertion into a socket with another pin assignment may damage the emCON-MX6 module and the carrier board.

Most of the pins are directly connected with the processor i.MX6x.

Pin	Signal	Interface	Signal	Pin
1E20	GND	Power Supply	VCC_5V	**2E20**
1E19	GND		VCC_5V	**2E19**
1E18	GND		VCC_5V	**2E18**
1E17	GND		VCC_5V	**2E17**
1E16	GND		VCC_5V	**2E16**
1E15	GND		VCC_5V	**2E15**
1E14	GND		VCC_5V	**2E14**
1E13	GND		VCC_5V	**2E13**
1E12	GND		VCC_5V	**2E12**
1E11	GND		VCC_5V	**2E11**
1E10	BAT		VCC_STANDBY	**2E10**
1E9	BOOT_MODE_3	Manufacturing / MISC	TAMPER	**2E9**
1E8	BOOT_MODE_2		POWER_ON_BASE	**2E8**
1E7	BOOT_MODE_1		IRQ_TOUCH1#	**2E7**
1E6	JTAG_RESET#		IRQ_TOUCH2#	**2E6**
1E5	JTAG_MOD		IRQ_1	**2E5**
1E4	JTAG_TRST#		IRQ_2	**2E4**
1E3	JTAG_TMS		IRQ_3	**2E3**
1E2	JTAG_TDO		RESO#	**2E2**
1E1	JTAG_TDI		RESI#	**40**

1	JTAG_RTCK			POWERFAIL#	2
3	JTAG_VCC			SUSPEND#	4
5	JTAG_TCK			ON_OFF#	6
7	GND	POWER		WAKEUP#	8
9	UART-A_RXD	UART-A		PWM_FAN	10
11	UART-A_TXD		POWER	GND	12
13	n/c		UART-C	UART-C_RXD	14
15	n/c			UART-C_TXD	16
17	UART-B_RXD	UART-B	UART-D	UART-D_RXD	18
19	UART-B_TXD			UART-D_TXD	20
21	UART-B_RTS		UART-E	UART-E_RXD	22
23	UART-B_CTS			UART-E_TXD	24
25	GND	POWER		GND	26
27	GPIO_1	GPIOs	PCI Express	PCIE_DISABLE#	28
29	GPIO_2			PCIE_RESET#	30
31	GPIO_3			PCIE_CLK1_P	32
33	GPIO_4			PCIE_CLK1_N	34
35	GPIO_5			GND	36
37	GPIO_6			PCIE_RX1_P	38
39	GPIO_7			PCIE_RX1_N	40
41	GPIO_8			PCIE_TX1_P	42
43	GND	POWER		PCIE_TX1_N	44
45	LCD_D23	RGB IF		GND	46
47	LCD_D22			PCIE_RX2_P	48
49	LCD_D21			PCIE_RX2_N	50
51	LCD_D20			PCIE_TX2_P	52
53	LCD_D19			PCIE_TX2_N	54
55	LCD_D18			GND	56
57	LCD_D17			PCIE_CLK2_P	58
59	LCD_D16			PCIE_CLK2_N	60
61	LCD_D15	RGB IF	PCI Express	GND	62

63	LCD_D14			PCIE_RX3_P	**64**
65	LCD_D13			PCIE_RX3_N	**66**
67	LCD_D12			PCIE_TX3_P	**68**
69	GND			PCIE_TX3_N	**70**
71	LCD_D11			GND	**72**
73	LCD_D10			PCIE_RX4_P	**74**
75	LCD_D9			PCIE_RX4_N	**76**
77	LCD_D8			PCIE_TX4_P	**78**
79	LCD_D7			PCIE_TX4_N	**80**
81	LCD_D6		**POWER**	GND	**82**
83	LCD_D5			n/c	**84**
85	LCD_D4			n/c	**86**
87	LCD_D3		**CPI 2 Camera Input**	CPI2_CLK	**88**
89	LCD_D2			CPI2_HSYNC	**90**
91	LCD_D1			CPI2_VSYNC	**92**
93	LCD_D0			CPI2_D0	**94**
95	LCD_PIXCLK			CPI2_D1	**96**
97	LCD_HSYNC			CPI2_D2	**98**
99	LCD_VSYNC			CPI2_D3	**100**
101	LCD_DISP			CPI2_D4	**102**
103	LCD_BL_CTRL			CPI2_D5	**104**
105	LCD_BL_EN			CPI2_D6	**106**
107	LCD_PANEL_EN			CPI2_D7	**108**
109	CAN2_RX	**CAN 2**	**CAN 1**	CAN1_RX	**110**
111	CAN2_TX			CAN1_TX	**112**
113	GND	**POWER**	**POWER**	GND	**114**
115	SPI1_SCK	**SPI 1**	**SPI 2**	n/c	**116**
117	SPI1_CS0#			n/c	**118**
119	SPI1_MOSI/D0			n/c	**120**
121	SPI1_MISO/D1			n/c	**122**
123	SPI1_CS1#/D2			n/c	**124**
125	n/c				

The pins 126 - 132 are used for mechanical coding and not available as electrical pins.

133	CPI1_D0	**CPI1 Camera Input**	**MIPI_CSI-2 Camera Input**	MIPI_CSI-2_D0_P	**134**
135	CPI1_D1			MIPI_CSI-2_D0_N	**136**
137	CPI1_D2			MIPI_CSI-2_D1_P	**138**
139	CPI1_D3			MIPI_CSI-2_D1_N	**140**
141	CPI1_D4			MIPI_CSI-2_D2_P	**142**
143	CPI1_D5			MIPI_CSI-2_D2_N	**144**
145	CPI1_D6			MIPI_CSI-2_D3_P	**146**
147	CPI1_D7			MIPI_CSI-2_D3_N	**148**
149	CPI1_CLK			MIPI_CSI-2_CLK_P	**150**
151	CPI1_HSYNC			MIPI_CSI-2_CLK_N	**152**
153	CPI1_VSYNC		**POWER**	GND	**154**
155	GND	**POWER**	**I2C1**	I2C1_SCL	**156**
157	LVDS1_BL_CTRL	**LVDS1 Control**		I2C1_SDA	**158**
159	LVDS1_BL_EN			n/c	**160**
161	LVDS1_PANEL_EN			n/c	**162**
163	GND	**POWER**	**LVDS2**	LVDS2_D0_P	**164**
165	LVDS1_D0_P	**LVDS1**		LVDS2_D0_N	**166**
167	LVDS1_D0_N			LVDS2_D1_P	**168**
169	LVDS1_D1_P			LVDS2_D1_N	**170**
171	LVDS1_D1_N			LVDS2_D2_P	**172**
173	LVDS1_D2_P			LVDS2_D2_N	**174**
175	LVDS1_D2_N			LVDS2_D3_P	**176**
177	LVDS1_D3_P			LVDS2_D3_N	**178**
179	LVDS1_D3_N			LVDS2_CLK_P	**180**
181	LVDS1_CLK_P			LVDS2_CLK_N	**182**
183	LVDS1_CLK_N		**POWER**	GND	**184**
185	GND	**POWER**	**HDMI**	HDMI_CLK_P	**186**
187	SPDIF_IN	**SPDIF**		HDMI_CLK_N	**188**
189	SPDIF_OUT			HDMI_D0_P	**190**
191	I2S_RXD	**I2S Audio**		HDMI_D0_N	**192**
193	I2S_TXD			HDMI_D0_P	**194**
195	I2S_TXFS			HDMI_D0_N	**196**
197	I2S_TXC			HDMI_D0_P	**198**

199	I2S_RXFS **			HDMI_D0_N	**200**
201	I2S_RXC **		**POWER**	GND	**202**
203	n/c		**HDMI Control**	HDMI_HPD	**204**
205	SATA_RX_P	**SATA**		HDMI_CEC	**206**
207	SATA_RX_N			HDMI_SCL	**208**
209	SATA_TX_P			HDMI_SDA	**210**
211	SATA_TX_N		**POWER**	GND	**212**
213	GND	**POWER**		GND	**214**
215	USBOTG_ID	**USB OTG**	**USB Host**	USBH_D_P	**216**
217	USBOTG_D_P			USBH_D_N	**218**
219	USBOTG_D_N			USBH_VBUS	**220**
221	USBOTG_VBUS			USBH_OC#	**222**
223	USBOTG_OC#			USBH_PEN#	**224**
225	USBOTG_PEN#			n/c	**226**
227	n/c			n/c	**228**
229	n/c		**POWER**	GND	**230**
231	GND	**POWER**		n/c	**232**
233	n/c			n/c	**234**
235	n/c		**POWER**	GND	**236**
237	GND	**POWER**	**SD Card 2**	SDC2_CLK	**238**
239	SDC1_CLK	**SD Card 1**		SDC2_CMD	**240**
241	SDC1_CMD			SDC2_D0	**242**
243	SDC1_D0			SDC2_D1	**244**
245	SDC1_D1			SDC2_D2	**246**
247	SDC1_D2			SDC2_D3	**248**
249	SDC1_D3			SDC2_CD#	**250**
251	SDC1_CD#			SDC2_WP	**252**
253	SDC1_WP		**POWER**	GND	**254**
255	GND	**POWER**		n/c	**256**
257	GBE1_MDI0_P	**GB Ethernet**		n/c	**258**
259	GBE1_MDI0_N			n/c	**260**
261	GBE1_MDI1_P			n/c	**262**
263	GBE1_MDI1_N	**GB Ethernet**		n/c	**264**

265	GBE1_MDI2_P	**1**		n/c	**266**
267	GBE1_MDI2_N			n/c	**268**
269	GBE1_MDI3_P			n/c	**270**
271	GBE1_MDI3_N		**POWER**	GND	**272**
273	GND	**POWER**		n/c	**274**
275	GBE_1_LED_10_100#	**GB Ethernet 1 Control**		n/c	**276**
277	GBE_1_LED_1000#***			n/c	**278**
279	GBE_1_TRAFFIC#			n/c	**280**
281	n/c				

** I2S_RXFS is shorted with I2S_TXFS and I2S_RXC is shorted with I2S_TXC.

*** GBE_1_LED_1000# is shorted with GBE_1_LED_10_100#.

7 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	digital input
O	digital output
I/O	digital bidirectional
O(OD)	digital open drain output

PU xK	x KΩ pullup resistor
PD xK	x KΩ pulldown resistor
SR xR	x Ω series resistor
IPU xK	processor internal x KΩ pullup resistor
IPD xK	transistor internal x KΩ pulldown resistor

7.1 J1, emCON Connector

Name	i.MX6 Pad Name	GPIO	Direction	Add. Wiring at Reset	Volt	Max. Current	Description
Gigabit Ethernet 1							
SPEED_LED#			O(OD)	-	3,3V	20mA	100 Mbit indicator
GBE1_MDI0_P			A I/O	-	-	N/A	Diff. data pair 0 pos.
GBE1_MDI0_N			A I/O	-	-	N/A	Diff. data pair 0 neg.
GBE1_MDI1_P			A I/O	-	-	N/A	Diff. data pair 1 pos.
GBE1_MDI1_N			A I/O	-	-	N/A	Diff. data pair 1 neg.
GBE1_MDI2_P			A I/O	-	-	N/A	Diff. data pair 2 pos.

GBE1_MDI2_N			A I/O	-	-	N/A	Diff. data pair 2 neg.
GBE1_MDI3_P			A I/O	-	-	N/A	Diff. data pair 3 pos.
GBE1_MDI3_N			A I/O	-	-	N/A	Diff. data pair 3 neg.
GBE1_LED_1000#			O	-	3,3V	20mA	speed indicator (GBE1_LED_1000# and GBE1_LED_10_100# are shorted)
GBE1_LED_10_100#			O	-	3,3V	20mA	speed indicator (GBE1_LED_1000# and GBE1_LED_10_100# are shorted)
GBE1_LED_TRAFFIC#			O	-	3,3V	20mA	traffic indicator
USB Host							
USBH_PEN#	EIM_D31	GPIO3-31	O	PU 10K	3,3V	1mA	USB power enable signal for power switch
USBH_OC#	EIM_D30	GPIO3-30	I	PU 10K	3,3V	N/A	USB overcurrent signal from power switch
USBH_DP	USB_H1_DP		I/O	-	3,0V	N/A	Diff. data positive
USBH_DM	USB_H1_DN		I/O	-	3,0V	N/A	Diff. data negative
USB OTG							
USBOTG_ID	ENET_RX_ER	GPIO1_24	I	PD 12K1	3.3V	N/A	USB ID signal for OTG functionality
USBOTG_PEN#	GPIO1_8	GPIO1_8	O	-	3.3V	1mA	USB power enable signal for power switch
USBOTG_OC#	GPIO1_7	GPIO1_7	I	-	3.3V	N/A	USB overcurrent signal from power switch
USBOTG_VBUS	USB_OTG_VBUS		I	-	5V	N/A	VBUS detection
USBOTG_DP	USB_OTG_DP		I/O	-	3,0V	N/A	Diff. data positive
USBOTG_DM	USB_OTG_DN		I/O	-	3,0V	N/A	Diff. data negative
SATA							
SATA_TXP	SATA_TXP		A O	-	2,5V	1,75mA	P signal of diff. SATA transmitter
SATA_TXN	SATA_TXM		A O	-	2,5V	1,75mA	N signal of diff. SATA transmitter
SATA_RXP	SATA_RXP		A I	-	2,5V	1,75mA	P signal of diff. SATA receiver
SATA_RXN	SATA_RXM		A I	-	2,5V	1,75mA	N signal of diff. SATA receiver
PCI Express							
PCIE_RXP	PCIE_RXP		A I		2,5V	4mA	P signal of diff. PCIe receive data
PCIE_RXM	PCIE_RXM		A I		2,5V	4mA	N signal of diff. PCIe receive data

PCIE_TXP	PCIE_TXP		A O		2,5V	4mA	P signal of diff. PCIe transmit data
PCIE_TXM	PCIE_TXM		A O		2,5V	4mA	N signal of diff. PCIe transmit data
CLK1_P	CLK1_P		A O		2,5V	4mA	P signal of diff. PCIe clock
CLK1_N	CLK1_N		A O		2,5V	4mA	N signal of diff. PCIe clock
PCIE_RESET#	GPIO7_12	GPIO7_12	O	-	3,3V	1mA	Reset output for PCIe
PCIE_DISABLE#	EIM_A16	GPIO2_22	O	-	3,3V	1mA	Disable output for PCIe
UART							
UART-A_TXD	CSI0_DAT10	GPIO5_28	O	PU 10K	3,3V	1mA	UART1: transmit data
UART-A_RXD	CSI0_DAT11	GPIO5_29	I	IPU 100K	3,3V	N/A	UART1: receive data
UART-B_TXD	SD4_DAT7	GPIO2_15	O	PU 10K	3,3V	1mA	UART2: transmit data
UART-B2_RXD	SD4_DAT4	GPIO2_12	I	IPU 100K	3,3V	N/A	UART2: receive data
UART-B_RTS	SD4_DAT6	GPIO	O	IPU 100K	3,3V	1mA	UART2: modem control
UART-B_CTS	SD4_DAT5		I	IPU 100K	3,3V	N/A	UART2: modem control
UART-C_TXD	EIM_D24	GPIO3-24	O	PU 10K	3,3V	1mA	UART3: transmit data
UART-C_RXD	EIM_D25	GPIO3-25	I	IPU 100K	3,3V	N/A	UART3: receive data
UART-D_TXD	KEY_COL0	GPIO4-6	O	PU 10K	3,3V	1mA	UART4: transmit data
UART-D_RXD	KEY_ROW0	GPIO4-7	I	IPU 100K	3,3V	N/A	UART4: receive data
UART-E_TXD	KEY_COL1	GPIO4-8	O	PU 10K	3,3V	1mA	UART5: transmit data
UART-E_RXD	KEY_ROW1	GPIO4-9	I	IPU 100K	3,3V	N/A	UART5: receive data
CAN							
CAN1_TX	KEY_COL2	GPIO4-10	O	IPU 100K	3,3V	1mA	transmit data
CAN1_RX	KEY_ROW2	GPIO4-11	I	PU 10K	3,3V	N/A	receive data
CAN2_TX	KEY_COL4	GPIO4-14	O	IPU 100K	3,3V	1mA	transmit data
CAN2_RX	KEY_ROW4	GPIO4-15	I	PU 10K	3,3V	N/A	receive data
LCD (Graphic Display)							

LCD_PIXCLK	DI0_DISP_CLK	GPIO4-16	O	IPU 100K	3,3V	1mA	LCD data clock
LCD_DISP	DI0_PIN15	GPIO4-17	O	IPU 100K	3,3V	1mA	LCD data enable signal
LCD_VSYNC	DI0_PIN3	GPIO4-19	O	IPU 100K	3,3V	1mA	LCD frame sync output
LCD_HSYNC	DI0_PIN2	GPIO4-18	O	IPU 100K	3,3V	1mA	LCD line sync output
LCD_D0	DISP0_DAT0	GPIO4-21	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D1	DISP0_DAT1	GPIO4-22	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D2	DISP0_DAT2	GPIO4-23	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D3	DISP0_DAT3	GPIO4-24	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D4	DISP0_DAT4	GPIO4-25	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D5	DISP0_DAT5	GPIO4-26	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D6	DISP0_DAT6	GPIO4-27	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D7	DISP0_DAT7	GPIO4-28	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D8	DISP0_DAT8	GPIO4-29	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D9	DISP0_DAT9	GPIO4-30	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D10	DISP0_DAT10	GPIO4-31	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D11	DISP0_DAT11	GPIO5-5	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D12	DISP0_DAT12	GPIO5-6	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D13	DISP0_DAT13	GPIO5-7	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D14	DISP0_DAT14	GPIO5-8	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D15	DISP0_DAT15	GPIO5-9	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D16	DISP0_DAT16	GPIO5-10	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D17	DISP0_DAT17	GPIO5-11	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D18	DISP0_DAT18	GPIO5-12	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D19	DISP0_DAT19	GPIO5-13	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D20	DISP0_DAT20	GPIO5-14	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D21	DISP0_DAT21	GPIO5-15	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D22	DISP0_DAT22	GPIO5-16	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_D23	DISP0_DAT23	GPIO5-17	O	IPU 100K	3,3V	1mA	LCD colour data
LCD_PANEL_EN	SD4_CMD	GPIO7-9	O	IPU 100K	3,3V	1mA	LCD panel power enable
LCD_BL_EN	NAND_ALE	GPIO6-8	O	IPU 100K	3,3V	1mA	LCD backlight power enable
LCD_BL_CTRL	SD4_DAT1	GPIO2-9	O	IPU 100K	3,3V	1mA	LCD backlight brightness control (PWMO3)

LVDS 1							
LVDS1_CLK_P	LVDS0_CLK_P		O	-	2,5V	2,5mA	P signal of diff. LVDS clock
LVDS1_CLK_N	LVDS0_CLK_N		O	-	2,5V	2,5mA	N signal of diff. LVDS clock
LVDS1_TX0_P	LVDS0_TX0_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS1_TX0_N	LVDS0_TX0_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS1_TX1_P	LVDS0_TX1_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS1_TX1_N	LVDS0_TX1_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS1_TX2_P	LVDS0_TX2_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS1_TX2_N	LVDS0_TX2_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS1_TX3_P	LVDS0_TX3_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS1_TX3_N	LVDS0_TX3_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS1_PANEL_EN	SD4_CLK	GPIO7-10	O	IPU 100K	3,3V	1mA	LVDS panel power enable
LVDS1_BL_EN	NAND_WP#	GPIO6-9	O	IPU 100K	3,3V	1mA	LVDS backlight power enable
LVDS1_BL_CTRL	GPIO1-9	GPIO1-9	O	IPU 100K	3,3V	1mA	LVDS backlight brightness control (PWMO1)
LVDS 2							
LVDS2_CLK_P	LVDS1_CLK_P		O	-	2,5V	2,5mA	P signal of diff. LVDS clock
LVDS2_CLK_N	LVDS1_CLK_N		O	-	2,5V	2,5mA	N signal of diff. LVDS clock
LVDS2_TX0_P	LVDS1_TX0_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS2_TX0_N	LVDS1_TX0_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS2_TX1_P	LVDS1_TX1_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS2_TX1_N	LVDS1_TX1_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS2_TX2_P	LVDS1_TX2_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS2_TX2_N	LVDS1_TX2_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
LVDS2_TX3_P	LVDS1_TX3_P		O	-	2,5V	2,5mA	P signal of diff. LVDS data
LVDS2_TX3_N	LVDS1_TX3_N		O	-	2,5V	2,5mA	N signal of diff. LVDS data
HDMI							

HDMI_D2_P	HDMI_D2P		O		2,5V	4mA	P signal of diff. HDMI data
HDMI_D2_N	HDMI_D2M		O		2,5V	4mA	N signal of diff. HDMI data
HDMI_D1_P	HDMI_D1P		O		2,5V	4mA	P signal of diff. HDMI data
HDMI_D1_N	HDMI_D1M		O		2,5V	4mA	N signal of diff. HDMI data
HDMI_D0_P	HDMI_D0P		O		2,5V	4mA	P signal of diff. HDMI data
HDMI_D0_N	HDMI_D0M		O		2,5V	4mA	N signal of diff. HDMI data
HDMI_CLK_P	HDMI_CLKP		O		2,5V	4mA	P signal of diff. HDMI clock
HDMI_CLK_N	HDMI_CLKM		O		2,5V	4mA	N signal of diff. HDMI clock
HDMI_SCL	KEY_COL3	GPIO4-12	O	PU 2K2	3,3V	3mA	HDMI I^2C clock signal
HDMI_SDA	KEY_ROW3	GPIO4-13	I/O (OD)	PU 2K2	3,3V	3mA	HDMI I^2C data signal
HDMI_HDP	HDMI_HDP		I	IPU 100K	3,3V	N/A	HDMI hot plug detect signal
HDMI_CEC	HDMICEC		I/O	IPU 100K	3,3V	1mA	HDMI CEC signal
CPI1 (Camera Input)							
CPI1_D0	IPU_CSI0_D12	GPIO5-30	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_D1	IPU_CSI0_D13	GPIO5-31	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_D2	IPU_CSI0_D14	GPIO6-0	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_D3	IPU_CSI0_D15	GPIO6-1	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_D4	IPU_CSI0_D16	GPIO6-2	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_D5	IPU_CSI0_D17	GPIO6-3	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D6	IPU_CSI0_D18	GPIO6-4	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_D7	IPU_CSI0_D19	GPIO6-5	I	IPU 100K	3,3V	N/A	Video image input data
CPI1_PIXCLK	IPU_CSI0_PIXCLK	GPIO5-18	I	IPU 100K	3,3V	N/A	Video clock input
CPI1_HSYNC	IPU_CSI0_HSYNC	GPIO5-19	I	IPU 100K	3,3V	N/A	Video hsync input
CPI1_VSYNC	IPU_CSI0_VSYNC	GPIO5-21	I	IPU 100K	3,3V	N/A	Video vsync input
CPI2 (Camera Input)							
CPI2_D0	EIM_A17	GPIO2-21	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D1	EIM_D27	GPIO3-27	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D2	EIM_D26	GPIO3-26	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D3	EIM_D20	GPIO3-20	I	IPU 100K	3,3V	N/A	Video image input data

CPI2_D4	EIM_D19	GPIO3-19	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D5	EIM_D18	GPIO3-18	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D6	EIM_D16	GPIO3-16	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_D7	EIM_EB2	GPI03-30	I	IPU 100K	3,3V	N/A	Video image input data
CPI2_PIXCLK	EIM_D17	GPIO2-22	I	IPU 100K	3,3V	N/A	Video clock input
CPI2_HSYNC	EIM_EB3	GPIO2-31	I	IPU 100K	3,3V	N/A	Video hsync input
CPI2_VSYNC	EIM_D29	GPIO3-29	I	IPU 100K	3,3V	N/A	Video vsync input
MIPI CSI-2							
MIPI_CSI-2_D0_P	CSI_D0P		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D0_N	CSI_D0M		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D1_P	CSI_D1P		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D1_N	CSI_D1M		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D2_P	CSI_D2P		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D2_N	CSI_D2M		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D3_P	CSI_D3P		I		2,5V	N/A	Video image input data
MIPI_CSI-2_D3_N	CSI_D3M		I		2,5V	N/A	Video image input data
MIPI_CSI-2_CLK_P	CSI_CLK0P		I		2,5V	N/A	Video image input clock
MIPI_CSI-2_CLK_N	CSI_CLK0M		I		2,5V	N/A	Video image input clock
SD Card Interface 1							
SDC1_D0	SD1_DAT0	GPIO1-16	I/O	IPU 100K	3,3V	1mA	SDC data
SDC1_D1	SD1_DAT1	GPIO1-17	I/O	IPU 100K	3,3V	1mA	SDC data
SDC1_D2	SD1_DAT2	GPIO1-19	I/O	IPU 100K	3,3V	1mA	SDC data
SDC1_D3	SD1_DAT3	GPIO1-21	I/O	IPU 100K	3,3V	1mA	SDC data
SDC1_CMD	SD1_CMD	GPIO1-18	I/O	IPU 100K	3,3V	1mA	CMD signal
SDC1_CLK	SD1_CLK	GPIO1-20	O	IPU 100K / SR 33R	3,3V	1mA	SDC Clock output
SDC1_CD#	GPIO_1	GPIO1-1	I	IPD 100K	3,3V	N/A	Card detect input
SDC1_WP	DI0_PIN4	GPIO4-20	I	IPU 100K	3,3V	N/A	Write protect input
SD Card Interface 2							

SDC2_D0	SD2_D0	GPIO1-15	I/O	IPU 100K	3,3V	1mA	SDC data
SDC2_D1	SDC_D1	GPIO1-14	I/O	IPU 100K	3,3V	1mA	SDC data
SDC2_D2	SD2_D2	GPIO1-13	I/O	IPU 100K	3,3V	1mA	SDC data
SDC2_D3	SD2_D3	GPIO1-12	I/O	IPU 100K	3,3V	1mA	SDC data
SDC2_CMD	SD2_CMD	GPIO1-11	I/O	IPU 100K	3,3V	1mA	CMD signal
SDC2_CLK	SD2_CLK	GPIO1-10	O	IPU 100K / SR 33R	3,3V	1mA	SDC Clock output
SDC2_CD#	GPIO_4	GPIO1-4	I	IPU 100K	3,3V	N/A	Card detect input
SDC2_WP	GPIO_2	GPIO1-2	I	IPU 100K	3,3V	N/A	Write protect input
SPI							
SPI_SS0#	EIM_RW		O	PU 10K	3,3V	20mA	Slave select output
SPI_SS1#	EIM_RW		O	PU 10K	3,3V	3mA	Slave select output
SPI_SCK	EIM_CS0	GPIO2-23	O	IPU 100K / SR 33R	3,3V	1mA	Clock output
SPI_MISO	EIM_OE	GPIO2-25	I	IPU 100K	3,3V	N/A	Input data from slave
SPI_MOSI	EIM_CS1	GPIO2-24	O	IPU 100K	3,3V	1mA	Output data to slave
I2C3							
I2C3_SCL	GPIO_3	GPIO1-3	I/O	PU 2K2	3,3V	3mA	I^2C clock signal
I2C3_SDA	GPIO_6	GPIO1-6	I/O (OD)	PU 2K2	3,3V	3mA	I^2C data signal
Audio SSI							
AUDIO_TXC	CSI0_DAT4	GPIO5-22	I/O	IPU 100K	3,3V	1mA	Sound bit clock
AUDIO_TXFS	CSI0_DAT6	GPIO5-24	I	IPU 100K	3,3V	N/A	Sound L/R signal
AUDIO_RXD	CSI0_DAT7	GPIO5-25	I	IPU 100K	3,3V	N/A	Sound serial input data
AUDIO_TXD	CSI0_DAT5	GPIO5-23	O	IPU 100K	3,3V	1mA	Sound serial output data
Audio SPDIF							
SPDIF_IN	GPIO_16	GPIO7-11	I	IPU 100K	3,3V	N/A	SPDIF sound serial input data
SPDIF_OUT	GPIO_19	GPIO4-5	O	IPU 100K	3,3V	1mA	SPDIF Sound serial output data
General Purpose I/O							

GPIO1	NANDF_D0	GPIO2-0	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO2	NANDF_D1	GPIO2-1	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO3	NANDF_D2	GPIO2-2	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO4	NANDF_D3	GPIO2-3	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO5	NANDF_D4	GPIO2-4	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO6	NANDF_D5	GPIO2-5	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO7	NANDF_D6	GPIO2-6	I/O	IPU 100K	3,3V	1mA	digital input / output
GPIO8	NANDF_D7	GPIO2-7	I/O	IPU 100K	3,3V	1mA	digital output only
Manufacturing							
JTAG_TCK	JTAG_TCK		I	PD 10K	3,3V	N/A	JTAG clock input
JTAG_TMS	JTAG_TMS		I	IPU 47K	3,3V	N/A	JTAG mode select input
JTAG_TRST#	JTAG_TRSTB		I	IPU 47K	3,3V	N/A	JTAG reset input
JTAG_TDI	JTAG_TDI		I	IPU 47K	3,3V	N/A	JTAG Data input
JTAG_TDO	JTAG_TDO		O		3,3V	1mA	JTAG Data output
JTAG_RTCK			O	PD 10K	3,3V	N/A	JTAG return TCK
JTAG_MOD	JTAG_MOD		I	PD 10K	3,3V	N/A	Mode selection JTAG/Boundary Scan
JTAG_RESET#	POR#		I	PU 10K	3,3V	N/A	JTAG reset
JTAG_VCC			O		3,3V		VCC reference
BOOT_MODE_1	BOOT_MODE0		I	PD 10K	3,3V	N/A	Boot Mode selection
BOOT_MODE_2	BOOT_MODE1		I	PU 10K	3,3V	N/A	Boot Mode selection
BOOT_MODE_3	-		I	PD 10K	3,3V	N/A	Boot Mode selection
Miscellaneous							
IRQ_1	NANDF_CLE	GPIO6-7	I	PU 10K	3,3V	N/A	Interrupt input
IRQ_2	NANDF_CS2	GPIO6-15	I	PU 10K	3,3V	N/A	Interrupt input
IRQ_3	NANDF_CS3	GPIO6-16	I	PU 10K	3,3V	N/A	Interrupt input
IRQ_TOUCH1#	GPIO1-5	GPIO1-5	I	PU 10K	3,3V	N/A	Interrupt input for touch controller
IRQ_TOUCH2#	EIM_BCLK	GPIO6-31	I	PU 10K	3,3V	N/A	Interrupt input for touch controller
POWERFAIL#	EIM_D23	GPIO3-23	I	PU 10K	3,3V	N/A	Power Fail interrupt
PWM_FAN	SD4_DAT2	GPIO2-10	O	IPU 100K	3,3V	1mA	PWM signal for fan control

RESI#	POR#	I	PU 10K	3,3V	N/A	Reset input from carrier board
RESO#		O	-	3,3V	20mA	Reset output to carrier board
POWER_ON_BASE		O	-	3,3V	20mA	Power enable signal for the 3,3V baseboard supply
SUSPEND#		O	-	3,3V	20mA	Power switching signal for VCC_5V
ON_OFF#		I	-	3,3V	N/A	Power management signal
WAKEUP#		I	-	3,3V	N/A	Power management signal
TAMPER	TAMPER	I	IPD 100K	3,3V	N/A	Tamper input for security features
Power Supply						
BAT		-	-	2,3V – 3,3V	N/A	Battery backup input for RTC
VCC_5V		-	-	-	N/A	+ 5V supply
VCC_STANDBY		-	-	-	N/A	+ 5V standby supply
GND		-	-	-	N/A	Ground

8 Technical Characteristics

8.1 Electrical Specifications

Supply voltage	5V, +/-5%
Current consumption	up to 3.0 A, depending on CPU and GPU load

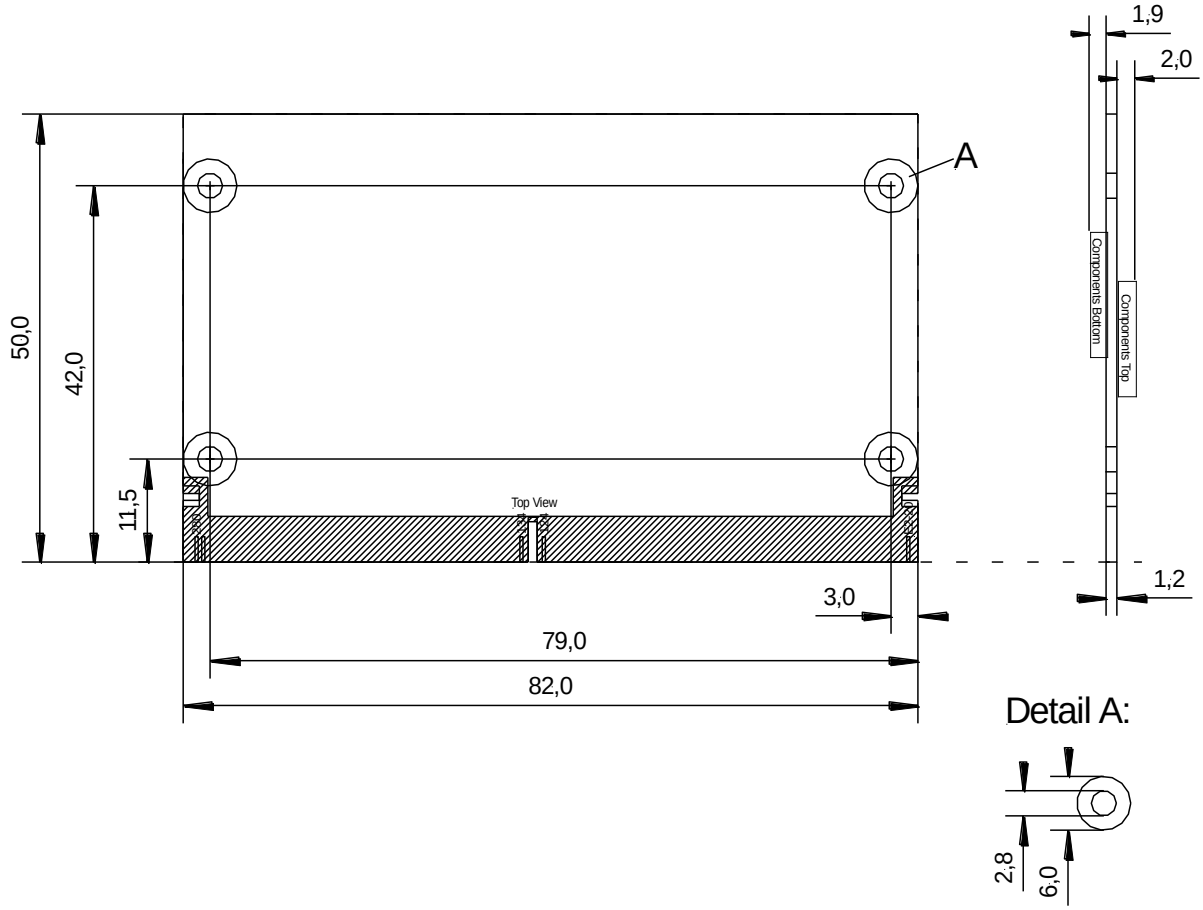
8.2 Environmental Specifications

Operating temperature	
Standard:	0 ... +70°C
Extended:	-40 ... +85°C
Storage temperature	-40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

8.3 Mechanical Specifications

Weight	approx. 19 g
Board	Glasepoxi FR-4, UL-listed, 10 layers
Dimensions	82.2 mm x 50.0 mm x 5.0 mm

9 Dimensional Drawing



10 References

[1] i.MX6x
Reference Manual
i.MX 6Dual/6Quad Applications Processor Reference Manual
IMX6DQRM Rev. D, 08/2012
Freescale semiconductor

[2] i.MX6x
Datasheet
i.MX 6Dual/6Quad Applications Processors for Consumer Products
IMX6DQCEC Rev. 0, 09/2012
i.MX 6Dual/6Quad Automotive and Infotainment Applications Processors
IMX6DQAEC Rev. C, 09/2012
Freescale semiconductor