emCON-RZ/G1E - Hardware Manual

Hardware Manual

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emtrion GmbH

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1	05.12.16/We	First release

Contents

1 Introduction

The emCON-RZ/G1E module is a CPU board of emtrion's emCON-family based on the RZ/G1E processor from Renesas.

The RZ/G1E processor is a multi chip module which incorporates two Cortex™-A7 MPCore™ cores. The cores run up to 1.0 GHz and are accompanied by a variety of functions required for rich graphics and industrial applications. These functions include a 3D graphics accelerator, video processing unit, USB 2.0 controllers, 1Gb- and 100MBitEthernet interface, CAN interface and others.

All interfaces are accessible through a 315 pin MXM type III edge connector. The pin assignment is defined by emtrion's emCON standard, which ensures a pin-to-pin compatibility within all emCON CPU modules.

The following table lists the features and interfaces of the emCON-RZ/G1E processor module:

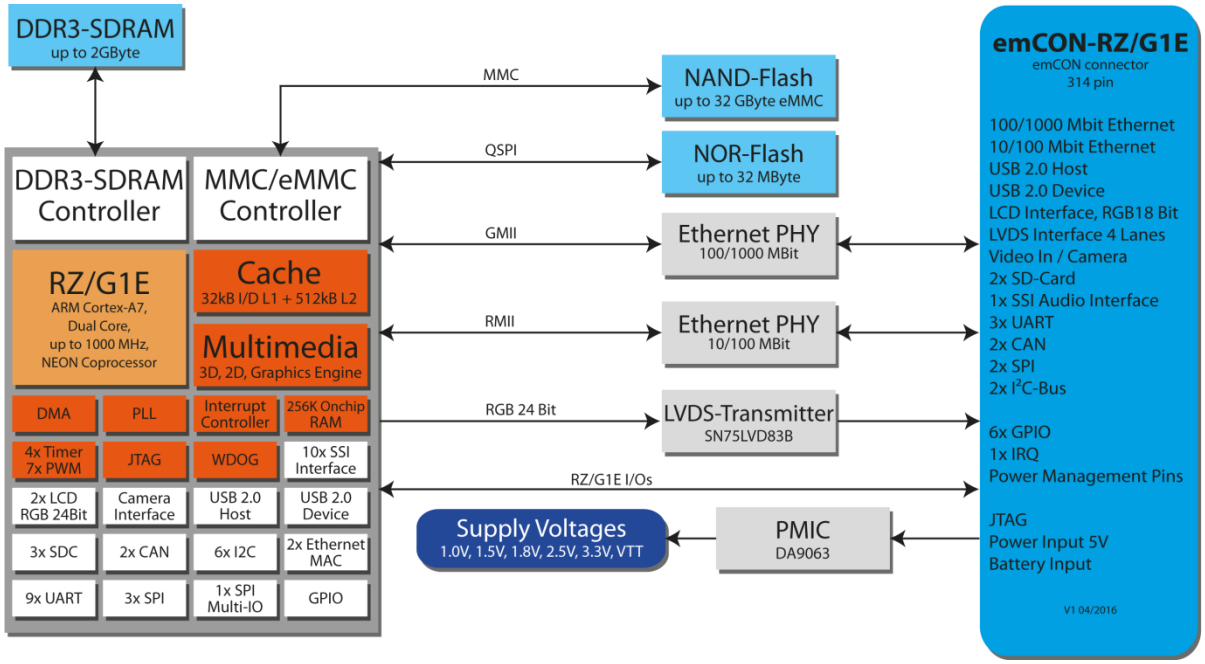
emCON-RZ/G1E
1 GByte DDR3-1333 RAM
up to 32GB eMMC NAND Flash
1 x 100 MBit Ethernet[1)] and 1 x 1000 Mbit Ethernet
1 x USB 2.0 Host
1 x USB 2.0 Device
1 x LCD Interface 18bit max. 1080p (1920x1080)
1 x LVDS 24bit max. 1080p (1920x1080)
1 x Video In, 8 bit [1)]
1 x SSI Audio
2 x SD Card
2 x CAN (LVTTL)
3 x UART (LVTTL)
2 x SPI
2 x I2C
6 x GPIO
RTC, battery backed
JTAG

[1)] Only one interface at the same time available: 100 MBit Ethernet or 1x Video In

The module is available in commercial temperature range 0°C to 70°C and in extended temperature range -40°C to 85°C.

2 Block Diagram

The following figure shows the block diagram of the emCON-RZ/G1E.



3 Handling Precautions

Please read the following notes prior to installing the processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The module does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatically discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The emCON-RZ/G1E module is based on the processor RZ/G1E from Renesas [1]. It incorporates two Cortex™-A7 cores which run at up to 1.0 GHz. In addition to the CPU cores with their NEON™/VFPv4 extension and L1 and L2 Caches, the processor provides a lot of peripheral functions such as:

- DDR3-1333 SDRAM controller
- NAND Flash controller
- 100/1000 Mb Ethernet MAC
- 10/100 Mb Ethernet MAC
- Image Processing Units which includes
    - 2 x display units for TFT displays with RGB; resolutions up to 1080p (1920x1080) @60Hz and 24 bpp are supported
    - 3D graphics engine: Imagination Technologies PowerVR Series5 SGX540 (260 MHz)
    - 2D graphics rendering function
    - 2 channel video input module
    - Video processing unit
- USB 2.0 Host only with high-speed mode
- USB 2.0 Host/Function with high-speed mode
- 3 x SD Card Host controller
- Audio interface with I2S format
- 2 x CAN controller
- 9 x UART with up to 128 byte FIFO
- 6 x I2C bus interface
- 3 x SPI interface
- 1 x QSPI
- Watchdog timer
- JTAG debug interface

Further details of the processor can be found in the RZ/G1E Reference Manual [1].

4.1.1 Processor Clocks

The processor is clocked by a 20 MHz main clock from a quartz crystal. Three internal PLLs multiply the 20 MHz clock input to the internally needed clocks. All clocks within the processor are derived from theses frequencies, via various software configurable dividers.

The core clock (PLL1) can be up to 1.0 GHz. This core clock can be varied according to power management needs. More information about the RZ/G1E clock system is described in the CCM chapter of the RZ/G1E Reference Manual [1].

4.1.2 Mode Settings

The processor mode is configured by 24 configuration pins that are sampled at the end of reset. All bits are fixed on the board.

4.2 DDR3 SDRAM

The module incorporates up to 2 GByte DDR3 SDRAM which are addressed as 32 bits x 1 channel. The RAMs are clocked with 666 MHz (DDR3-1333 mode).

RAM size	Start address	End address
1GB	0x00 4000 0000	0x00 7FFF FFFF

Please contact emtrion GmbH for your required RAM size.

4.3 NOR-Flash

A 16 MByte QSPI NOR Flash is connected to the QSPI interface of the RZ/G1E processor. This is the standard boot device and cannot be changed.

The clock rate of the interface is limited to 48.75 MHz by the processor.

4.4 eMMC

To store the operating system and application data, normally a 4 GByte eMMC is available on the emCON-RZ/G1E module. It is connected to the MMC interface of the RZ/G1E using 8 data lines.

The capacity of the eMMC can be between selected between 4 GB and 32 GB depending on the ordering code.

Please contact emtrion GmbH for your required eMMC capacity.

4.5 SD-Card Interface

The RZ/G1E includes three SD Card Host interfaces. Two of them (SDHI0 and SDHI1) are connected to the SD Card interfaces SDC1 and SDC2 of the emCON connector.

The signaling voltage of both SD Card interfaces can be switched individually between 1.8 V and 3.3 V by the GPIOs GP1_21 (SDC1 on emCON connector J1) and GP1_20 (SDC2 on emCON connector J1) . A low level selects 1.8 V and a high level selects 3.3 V.

Watch that the active high Write Protect inputs of both interfaces are pulled high at the CPU module. The pin must be pulled low externally if a µSD socket is connected since these sockets do not incorporate a write protect switch.

4.6 DIP Switches / Multiplexer

The 100Mbit Ethernet interfaces of the RZ/G1E shares the same pins with the VIN1 8-bit camera interface of the CPU. To have both interfaces available on the emCON-RZ/G1E board, a multiplexer is user to switch one of the two interfaces to the emCON-Connector J1. Therefore only one of the two interfaces is available at the same time.

The DIP switches SW1 on the emCON-RZ/G1E board are used to switch between Ethernet-AVB and the VIN1 interface. The following table describes how to select the desired interface.

SW1-1	SW1-2	Selected Interface
(don't care)	ON	VIN1
(don't care)	OFF	100MBit Ethernet

4.7 1GBit Ethernet

The RZ/G1E processor incorporates a 1GBit Ethernet interface, called Ethernet AVB. An Ethernet PHY KSZ9031MNX from Micrel is used to connect the Ethernet AVB interface to the GBit Ethernet interface 1 (GBE1) of the emCON connector. The PHY address is set to 0.

The LED signals for speed and traffic are connected to the appropriate pins.

An appropriate 1:1 transformer with a 100nF capacitor to GND at each center tap pin must be added externally. The center tap pin shall not be supplied with 3.3V!

The emCON pin GBE1_LED_10_100# and GBE1_LED_1000# are both connected to the LED1 pin of the Ethernet PHY and light if a link is established. Therefore the link speed has to be determined by software.

The emCON pin GBE1_LED_TRAFFIC# is connected to the LED2 pin of the Ethernet PHY and indicates if data is transferred ("blinking light" = traffic).

The 100MBit Ethernet Phy can be reset either by the global reset signal RESO# or by the GP1_16. A low signal at this pin resets the 1GBit Ethernet Phy.

4.8 10Mbit/100Mbit Ethernet

The RZ/G1E processor incorporates a 10MBit/100MBit Ethernet interface, called Ethernet MAC. An Ethernet PHY LAN8720A from Microchip is used to connect the Ethernet MAC interface to the GBit Ethernet interface 2 (GBE2) of the emCON connector. The PHY address is set to 1. The RMII interface is used for communication between the MAC and the PHY.

Note: The Ethernet MAC interface shares the same pins with the VIN1 8 bit camera interface. Therefore the Ethernet MAC has to be switched to the emCON connector J1 via a multiplexer. See chapter "DIP Switches / Multiplexer" for the correct DIP-Switch setting for the Ethernet MAC interface.

The Ethernet signal lines GBE2_MDI0_P, GBE2_MDI0_N (for TX) and GBE2_MDI1_P, GBE2_MDI1_N (for RX) as well as two status signals GBE2_LED_10_100# and GBE2_LED_TRAFFIC# that serve to indicate the link status and the transfer speed are connected to the emCON connector J1. An appropriate 1:1 transformer with a center tap sourced by 3.3V, must be added externally.

The signal GBE2_LED_TRAFFIC# indicates if data packages are transferred. ("0" = traffic). The GBE2_LED_TRAFFIC# signal is an open Drain output signal.

The signal GBE2_LED_10_100# indicates if the data is transferred with 100Mbit/s. ("0" = 100Mbit/s). The GBE2_LED_10_100# signal is an open Drain output signal.

The 100MBit Ethernet Phy can be reset either by the global reset signal RESO# or by the GP1_17. A low signal at this pin resets the 100MBit Ethernet Phy.

4.9 USB 2.0

The RZ/G1E processor incorporates a USB 2.0 Host interface (USB1) and a USB 2.0 Host/Function interface (USB0). Both USB 2.0 interfaces are connected to the emCON connector.

The USB1 interface of the RZ/G1E is connected to the USB 2.0 Host interface of the emCON connector. The pin GP5_26 of the RZ/G1E processor is used as active high USB Host Power Enable output. The signal is inverted and connected to the active low signal USBH_PEN# of the emCON interface. The pin GP5_27 is the corresponding overcurrent input of the USB Host interface.

The USB0 interface of the RZ/G1E is connected to the USB OTG interface of the emCON connector. The interface USB0 is configured to Function. The pin GP5_25 becomes the VBUS detection input.

4.10 Graphic Displays

Two display unit interfaces DU0 and DU1 are available at the RZ/G1E processor. The DU0 and DU1 interface are standard 24 bpp RGB interface with LVTTL signals. Both display units can display the same image on both monitors or fully independent images.

The maximum resolution of both display units is 1080 x 1920 pixels which is FullHD. A frame rate of 60 fps at that resolution would demand a 148.5 MHz pixel clock. Since the clock is derived from the internal processor clock ZXϕ with 520MHz only 130 MHz can be selected.

4.10.1 RGB Interface

DU0 of the RZ/G1E is connected to the RGB interface of emCON connector. Only the upper 18 colour bits and a set of control lines are available at the emCON connector. The backlight control signal LCD_BL_CTRL is driven by the pin GP0_21/PWM4_B of the RZ/G1E processor. The pin LCD_BL_EN is driven by GP1_23 and the pin LCD_PANEL_EN is driven by GP1_24.

The following table describes the function of the data and control lines.

Signal	Description
LCD_D[17:0]	18 bit color data
LCD_VSYNC	Vertical synchronization signal
LCD_HSYNC	horizontal synchronization signal
LCD_DE	Data enable signal, if active colour data are valid
LCD_PCLK	Display clock
LCD_PANEL_EN	Display power enable signal, GP1_24
LCD_BL_EN	Backlight power enable signal, GP1_23
LCD_BL_CTRL	PWM signal to control the backlight, GP0_21/PWM4_B

The following table shows the RGB colour mapping of the pins LCD_D[23:0] at the emCON connector.

LCD_D[23:0]	RGB666 (18bit)
LCD_D0	B2
LCD_D1	B3
LCD_D2	B4
LCD_D3	B5
LCD_D4	B6
LCD_D5	B7
LCD_D6	G2
LCD_D7	G3
LCD_D8	G4
LCD_D9	G5
LCD_D10	G6
LCD_D11	G7
LCD_D12	R2
LCD_D13	R3
LCD_D14	R4
LCD_D15	R5
LCD_D16	R6
LCD_D17	R7
LCD_D18	n/c
LCD_D19	n/c
LCD_D20	n/c
LCD_D21	n/c
LCD_D22	n/c
LCD_D23	n/c

4.10.2 LVDS Interface

DU1 of the RZ/G1E is connected to a serializer to convert the 24Bit RGB signal into an LVDS signal with 4 differential data lanes. The used serializer is SN75LVDS83B from TI. The LVDS signal is available on the LVDS1 interface of the emCON connector.

The backlight control signal LVDS1_BL_CTRL is driven by the pin GP0_13/PWM2_C of the RZ/G1E processor. The pin LVDS1_BL_EN is driven by GP0_22 and the pin LVDS1_PANEL_EN is driven by GP0_27.

The following table describes the signals of LVDS1 interface:

Signal	Description
LVDS1_CLK_P/N	Differential LVDS clock pair
LVDS1_CH[3:0]_P/N	Differential LVDS data signal pairs
LVDS1_PANEL_EN	Display power enable signal, GP0_27
LVDS1_BL_EN	Backlight power enable signal, GP0_22
LVDS1_BL_CTRL	PWM signal to control the backlight, GP0_13/PWM2_C

The following table shows the pixel data assignment from the RGB interface DU1 to the LVDS signal pairs.

Signal	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_CH0	G2	R7	R6	R5	R4	R3	R2
LVDS_CH1	B3	B2	G7	G6	G5	G4	G3
LVDS_CH2	DE	VS	HS	B7	B6	B5	B4
LVDS_CH3	CTL	B1	B0	G1	G0	R1	R0

4.11 Video Input VIN1

The emCON-RZ/G1E processor incorporates three video input units which can be used with different video sources, such as video CODECs or CMOS camera modules.

Only the interface VIN1 of the RZ/G1E processor is available at the CPI1 interface pins of the emCON connector. The second parallel interface CPI2 and the serial MIPI interface CSI2 of the emCON connector are unused. This is limited by the pin multiplexing configuration.

Note: The video input interface VIN1 shares the same pins with the Ethernet MAC interface. Therefore the video input VIN1 of the RZ/G1E has to be switched to the emCON connector J1 via a multiplexer. See chapter “DIP Switches / Multiplexer“ for the correct DIP-Switch setting for the VIN1 interface.

4.12 Audio Interface

The audio interfaces SSI0129 and SSI4 of the RZ/G1E processor are connected to the I2S audio interface pins of the emCON connector. SSI0129 is the output channel, SSI4 is the input channel. Both channels can be operated independently with different data format and clock rates.

An external audio CODEC with I2S interface can directly be connected to the interface pins.

Since the audio interface clocks are derived from the internal processor clock M2ϕ with 195 MHz they do not fit perfectly to the needed audio frequencies. For example the frequency error at 44.1 kHz sample rate is 0.13%. To get exact audio frequencies an external audio clock source can be connected to the emCON pin I2S_MCLK which is connected to the pin AUDIO_CLKA of the RZ/G1E processor.

4.13 Serial Ports

The emCON-RZ/G1E processor has six serial ports with 64 byte FIFO, SCIF, and additionally three high speed serial ports HSCIF with 128 byte FIFO. All ports have modem control lines RTS and CTS.

At the emCON connector 3 UART interfaces are specified, one of them incorporate modem control lines.

The following table shows the usage of the UART interfaces:

RZ/G1E peripheral	emCON interface	Modem Control
HSCIF2	UART_A	RTS/CTS
SCIF5	UART_C	not available
SCIF4	UART_D	not available

UARTA is used as standard debug and communication interface (Terminal).

4.14 I²C Interfaces

The RZ/G1E processor incorporates six I²C interfaces. The interfaces I2C2 and I2C3 of the processor RZ/G1E are connected to the interfaces I2C1 and I2C2 of the emCON connector.

RZ/G1E peripheral	emCON interface
I2C2	I2C1
I2C3	I2C2

The interfaces at the emCON connector operate with 400 kHz clock and have 2K2 pull-up resistors to 3.3 V.

The interface I2C0 is used on board to connect the PMIC to the processor. The internally used I2C0 component on the module has the following characteristics:

Function	Device	Interface	High Level	I²C Address (7bit)
PMIC	DA9063	I2C0	3.3 V	0x58

4.15 SPI Interfaces

The RZ/G1E processor incorporates three SPI interfaces.

The interface MSIOF1 of the RZ/G1E processor is connected to the SPI1 interface of the emCON connector and the interface MSIOF2 is connected to the SPI2 interface. Each SPI interface has one chip-select available on the emCON connector.

RZ/G1E peripheral	RZ/G1E Chip-selects	emCON interface	emCON Chip-selects
MSIOF1	MSIOF1_SS1	SPI1	SPI1_CS0#
MSIOF2	MSIOF2_SS1	SPI2	SPI2_CS0#

4.16 CAN

The RZ/G1E processor incorporates two CAN controllers, which comply with the ISO11898-1 specification. The CAN protocol specification 2.0B, with standard and extended message frames, are supported. The maximum baud rate is 1Mbps.

The TX and RX signals of both interfaces are routed to the emCON connector as LVTTL signals. CAN transceivers must be added externally.

4.17 General Purpose I/Os

The emCON interface provides six dedicated GPIOs which are directly connected to the CPU. The following table shows the signal connections:

emCON Signal	RZ/G1E Pin	Direction
GPIO_1	GP0_1	In/Out
GPIO_2	GP0_2	In/Out
GPIO_3	GP5_4	In/Out
GPIO_4	GP4_31	In/Out
GPIO_5	GP4_26	In/Out
GPIO_6	GP4_29	In/Out

All signals have LVTTL level and can drive up to +/-8 mA when configured as output.

4.18 PWM

The RZ/G1E includes seven PWM timers. Three of them are used at the emCON connector:

emCON Signal	PWM Channel	Remark
LCD_BL_CTRL	GP0_21/PWM4_B	Backlight dimming
LVDS1_BL_CTRL	GP0_13/PWM2_C	Backlight dimming
PWM_FAN	GP0_10/PWM5_C	Fan control

The signal level of each PWM pin is 3,3V.

4.19 Status LED

A bicolour LED is connected to the pins GP0_23 and GP1_3 of the RZ/G1E. If GP0_23 is high the LED is lighting green, if GP1-3 is high the LED is lighting red. If both pins are high the LED is lighting yellow.

4.20 Interrupts

The RZ/G1E processor has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor. The interrupts can be configured to be edge triggered on rising or falling edge or to be level sensitive on high or low level.

The emCON connector specifies six interrupt inputs. Two of them are reserved for touch interface controllers. Three inputs are generous interrupt inputs. The last interrupt input is provided as power fail input.

The following table shows the interrupt connections of the emCON connector:

Signal	RZ/G1E Pin
IRQ_1	**NMI**
IRQ_TOUCH1#	**IRQ4/GP0_0**
IRQ_TOUCH2#	**IRQ3/GP0_7**

The interrupt inputs at the emCON connector are pulled high by 10 kΩ resistors.

4.21 Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the 3.3 V board supply voltage. If the voltage is too low a module reset is asserted. After the supply has risen above 2.93 V the reset is kept active for another 200 ms.
- The active low signal RESI# of the emCON connector causes a reset that is kept active for another 200 ms after RESI# became high.
- The signal JTAG_RESI# of the emCON connector directly causes a reset.
- The GPIO GP3_27 of the RZ/G1E can directly cause a reset if the pin is set to output low.
- A processor internal SW or Watchdog reset is available at a processor pin, if the pin function SYSTEM_RST is enabled.

Except for the JTAG-Reset (JTAG_RESI#) All resets are hardware resets of the whole board. All resets issue a processor cold reset. The duration of the reset signal is min. 200ms. For resetting external devices the reset signal is available as an output (RESO#) at the emCON connector.

4.22 Power Supply

The typical power consumption is between 0.4A-1.6A at +5V, +/- 5%, depending on the running software tasks, which must be supplied via the emCON connector.

All on board supply voltages that are required for the processor and the other components are generated on board by the Power Management Chip DA9063 from Dialog Semiconductor.

The output voltages of the PMICs can be configured via the I^2C interface I2C0. The 7-bit I^2C address of the PMIC DA9063 is 0x5A.

4.22.1 Power Management Signals

VCC_5V, VCC_STANDBY
VCC_5V is the main supply input for the module. To keep only parts of the PMIC alive in power down states a second supply VCC_STANDBY is provided. This voltage only supplies parts of the PMIC DA9063L with little current consumption.

The output signal SUSPEND# of the emCON connector is provided to switch off the main supply VCC_5V in power down states. The switch must be realized on the carrier board. If no power management is needed, VCC_STANDBY and VCC_5V can be connected.

POWER_ON_BASE:
If the 3.3 V supply of the CPU module is switched off by power management, it must be ensured that no external peripherals with 3.3 V interface drive input pins. Otherwise unintended current flow might happen across the data lines.

The signal POWER_ON_BASE is provided to switch off external components with 3.3 V supply. The signal is high while the 3.3 V supply on the module is active. Otherwise the signal is low. The power switch must be realized on the carrier board.

POWERFAIL#
The signal POWERFAIL# is an input to signalize a power fail condition. The signal is connected to the GP3_31 pin of the RZ/G1E processor.

ON_OFF#
The signal ON-OFF# can be used to switch the PMIC into power down and back to normal operating mode. This pin must be driven by an open collector circuit. A circuit on the module causes a low pulse every time when VCC_STANDBY powers up to cause an automatic start of the module.

BAT:
The pin BAT at the emCON connector is used as battery input for the RTC's backup power supply. The typical power consumption of the RTC at the BAT pin is < 1.0 µA.

5 emCON Interface

All interface signals of the board are available at the emCON connector.

The emCON interface is a 314 pos MXM connector. These sockets are available from various manufacturers.

The pin assignment is emtrion specific and match for the most needs of interfaces for actual embedded designs. Depending on the features of the CPUs every emtrion CPU module will use a subset of the emCON connector. More details can be found in emtrion's emCON specification.

Usage details of the connector and its electrical and mechanical characteristics can be found further down in this document.

Notes:

The pin assignment of the emCON connector is ONLY compatible with devices of emtrion's emCON-family. Insertion into a socket with another pin assignment may damage the emCON-RZ/G1E module and the carrier board.

Most of the pins are directly connected with the processor RZ/G1E.

6 Pin Assignments

6.1 J1, emCON Connector

Type MXM, 314 pos
Compatible carrier board connector: Aces 91782-3140M-001

Pin	Signal	Interface		Signal	Pin
1E20	GND	Power Supply		VCC_5V	2E20
1E19	GND			VCC_5V	2E19
1E18	GND			VCC_5V	2E18
1E17	GND			VCC_5V	2E17
1E16	GND			VCC_5V	2E16
1E15	GND			VCC_5V	2E15
1E14	GND			VCC_5V	2E14
1E13	GND			VCC_5V	2E13
1E12	GND			VCC_5V	2E12
1E11	GND			VCC_5V	2E11
1E10	BAT			VCC_STANDBY	2E10
1E9	n/c	Manufacturing	MISC	n/c	2E9
1E8	n/c			POWER_ON_BASE	2E8
1E7	n/c			IRQ_TOUCH1#	2E7
1E6	JTAG_RESET#			IRQ_TOUCH2#	2E6
1E5	JTAG_MOD			IRQ_1	2E5
1E4	JTAG_TRST#			n/c	2E4
1E3	JTAG_TMS			n/c	2E3
1E2	JTAG_TDO			RESO#	2E2
1E1	JTAG_TDI			RESI#	2E1
1	JTAG_RTCK			POWERFAIL#	2
3	1.8 V JTAG_VCC			SUSPEND#	4
5	JTAG_TCK			ON_OFF#	6
7	GND	POWER		n/c	8
9	UART-A_RXD	UART-A		PWM_FAN	10
11	UART-A_TXD		POWER	GND	12
13	UART-A_RTS		UART-C	UART-C_RXD	14
15	UART-A_CTS			UART-C_TXD	16
17	n/c	UART-B	UART-D	UART-D_RXD	18
19	n/c			UART-D_TXD	20
21	n/c		UART-E	n/c	22
23	n/c			n/c	24
25	GND	POWER		GND	26
27	GPIO_1	GPIOs	PCIe	n/c	28
29	GPIO_2			n/c	30
31	GPIO_3			n/c	32
33	GPIO_4			n/c	34
35	GPIO_5			n/c	36
37	GPIO_6			n/c	38

39	n/c			n/c	**40**
41	n/c			n/c	**42**
43	GND	**POWER**		n/c	**44**
45	n/c			GND	**46**
47	n/c			n/c	**48**
49	n/c			n/c	**50**
51	n/c			n/c	**52**
53	n/c			n/c	**54**
55	n/c			GND	**56**
57	LCD_D17			n/c	**58**
59	LCD_D16			n/c	**60**
61	LCD_D15			GND	**62**
63	LCD_D14			n/c	**64**
65	LCD_D13			n/c	**66**
67	LCD_D12			n/c	**68**
69	GND			n/c	**70**
71	LCD_D11			GND	**72**
73	LCD_D10			n/c	**74**
75	LCD_D9	**RGB IF**		n/c	**76**
77	LCD_D8			n/c	**78**
79	LCD_D7			n/c	**80**
81	LCD_D6		**POWER**	GND	**82**
83	LCD_D5		**RFU**	n/c	**84**
85	LCD_D4			n/c	**86**
87	LCD_D3			n/c	**88**
89	LCD_D2			n/c	**90**
91	LCD_D1			n/c	**92**
93	LCD_D0			n/c	**94**
95	LCD_PIXCLK			n/c	**96**
97	LCD_HSYNC		**CPI2 Camera**	n/c	**98**
99	LCD_VSYNC			n/c	**100**
101	LCD_DISP			n/c	**102**
103	LCD_BL_CTRL			n/c	**104**
105	LCD_BL_EN			n/c	**106**
107	LCD_PANEL_EN			n/c	**108**
109	CAN2_RX	**CAN2**	**CAN1**	CAN1_RX	**110**
111	CAN2_TX			CAN1_TX	**112**
113	GND	**POWER**	**POWER**	GND	**114**
115	SPI1_SCK			n/c	**116**
117	SPI1_CS0#			SPI2_CS0#	**118**
119	SPI1_MOSI	**SPI 1**	**SPI 2**	SPI2_MOSI	**120**
121	SPI1_MISO			SPI2_MISO	**122**
123	n/c			SPI2_SCK	**124**
125	n/c				
	The pins 126 - 132 are used for mechanical coding and not available as electrical pins.				
133	CPI1_D0	**CPI1 Camera**	**MIPI_CSI2**	n/c	**134**

135	CPI1_D1		Camera	n/c	136
137	CPI1_D2			n/c	138
139	CPI1_D3			n/c	140
141	CPI1_D4			n/c	142
143	CPI1_D5			n/c	144
145	CPI1_D6			n/c	146
147	CPI1_D7			n/c	148
149	CPI1_CLK			n/c	150
151	CPI1_HSYNC			n/c	152
153	CPI1_VSYNC		POWER	GND	154
155	GND	POWER	I2C1	I2C1_SCL	156
157	LVDS1_BL_CTRL	LVDS1 Control		I2C1_SDA	158
159	LVDS1_BL_EN		I2C2	I2C2_SCL	160
161	LVDS1_PANEL_EN			I2C2_SDA	162
163	GND	POWER	LVDS2	n/c	164
165	LVDS1_D0_P	LVDS1		n/c	166
167	LVDS1_D0_N			n/c	168
169	LVDS1_D1_P			n/c	170
171	LVDS1_D1_N			n/c	172
173	LVDS1_D2_P			n/c	174
175	LVDS1_D2_N			n/c	176
177	LVDS1_D3_P			n/c	178
179	LVDS1_D3_N			n/c	180
181	LVDS1_CLK_P			n/c	182
183	LVDS1_CLK_N		POWER	GND	184
185	GND	POWER	HDMI	n/c	186
187	n/c	SPDIF		n/c	188
189	n/c			n/c	190
191	I2S_RXD	I2S Audio		n/c	192
193	I2S_TXD			n/c	194
195	I2S_TXFS			n/c	196
197	I2S_TXC			n/c	198
199	I2S_RXFS			n/c	200
201	I2S_RXC		POWER	GND	202
203	ACLK		HDMI Control	n/c	204
205	n/c	SATA		n/c	206
207	n/c			n/c	208
209	n/c			n/c	210
211	n/c		POWER	GND	212
213	GND	POWER		GND	214
215	USBOTG_ID	USB OTG	USB Host	USBH DP	216
217	USBOTG_D_P			USBH DN	218
219	USBOTG_D_N			n/c	220
221	USBOTG_VBUS			USBH OC#	222
223	USBOTG_OC#			USBH PEN#	224
225	USBOTG_PEN#		USB3.0	n/c	226

227	n/c			n/c	**228**
229	n/c		**POWER**	GND	**230**
231	GND	**POWER**	**USB3.0**	n/c	**232**
233	n/c			n/c	**234**
235	n/c		**POWER**	GND	**236**
237	GND	**POWER**		SDC2 CLK	**238**
239	SDC1 CLK			SDC2 CMD	**240**
241	SDC1 CMD			SDC2 D0	**242**
243	SDC1 D0		**SD Card 2**	SDC2 D1	**244**
245	SDC1 D1	**SD Card 1**		SDC2 D2	**246**
247	SDC1 D2			SDC2 D3	**248**
249	SDC1 D3			SDC2 CD#	**250**
251	SDC1 CD#			SDC2 WP	**252**
253	SDC1_WP		**POWER**	GND	**254**
255	GND	**POWER**		n/c	**256**
257	GBE1 MDI0 P			n/c	**258**
259	GBE1 MDI0 N			n/c	**260**
261	GBE1 MDI1 P		**Ethernet2**	n/c	**262**
263	GBE1 MDI1 N	**Ethernet1**		GBE2 MDI1 N	**264**
265	GBE1 MDI2 P			GBE2 MDI1 P	**266**
267	GBE1 MDI2 N			GBE2 MDI0 N	**268**
269	GBE1 MDI3 P			GBE2 MDI0 N	**270**
271	GBE1 MDI3 N		**POWER**	GND	**272**
273	GND	**POWER**		ETH LED 10 100M#	**274**
275	GBE 1 LED 10 100#**		**Ethernet2**	n/c	**276**
277	GBE 1 LED 1000#**	**Ethernet1**		ETH LED TRA#	**278**
279	GBE 1 TRAFFIC#			n/c	**280**
281	n/c				

** GBE_1_LED_1000# is shorted with GBE_1_LED_10_100#.

7 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	digital input
O	digital output
I/O	digital bidirectional
O(OD)	digital open drain output

PU xK	x KΩ pullup resistor
PD xK	x KΩ pulldown resistor
SR xR	x Ω series resistor
IPU xK	processor internal x KΩ pullup resistor
IPD xK	transistor internal x KΩ pulldown resistor

7.1 J1, emCON Connector

Name	RZ/G1E Pin	GPIO	Direction	Termination	Volt	max. Current	Description
Gigabit Ethernet 1							
GBE1_MDI0_P	-	-	A I/O	-	-	N/A	Diff. data pair 0 pos.
GBE1_MDI0_N	-	-	A I/O	-	-	N/A	Diff. data pair 0 neg.
GBE1_MDI1_P	-	-	A I/O	-	-	N/A	Diff. data pair 1 pos.
GBE1_MDI1_N	-	-	A I/O	-	-	N/A	Diff. data pair 1 neg.
GBE1_MDI2_P	-	-	A I/O	-	-	N/A	Diff. data pair 2 pos.
GBE1_MDI2_N	-	-	A I/O	-	-	N/A	Diff. data pair 2 neg.
GBE1_MDI3_P	-	-	A I/O	-	-	N/A	Diff. data pair 3 pos.
GBE1_MDI3_N	-	-	A I/O	-	-	N/A	Diff. data pair 3 neg.
GBE1_LED_1000#	-	-	O	-	3,3V	20mA	speed indicator (GBE1_LED_1000# and GBE1_LED_10_100# are shorted)
GBE1_LED_10_100#	-	-	O	-	3,3V	20mA	speed indicator (GBE1_LED_1000# and GBE1_LED_10_100# are shorted)
GBE1_LED_TRAFFIC#	-	-	O	-	3,3V	20mA	traffic indicator
Gigabit Ethernet 2							
GBE2_MDI0_P	-	-	A I/O	-	-	N/A	Diff. data pair 0 pos.
GBE2_MDI0_N	-	-	A I/O	-	-	N/A	Diff. data pair 0 neg.
GBE2_MDI1_P	-	-	A I/O	-	-	N/A	Diff. data pair 1 pos.
GBE2_MDI1_N	-	-	A I/O	-	-	N/A	Diff. data pair 1 neg.
GBE2_LED_10_100#	-	-	O	-	3,3V	20mA	speed indicator
GBE2_LED_TRA#	-	-	O	-	3,3V	20mA	traffic indicator
USB Host							
USBH_PEN#	T21	GPIO5_26	O	-	3,3V	4mA	USB power enable signal for power switch
USBH_OC#	T22	GPIO5_27	I	PU 10K	3,3V	N/A	USB overcurrent signal from power switch
USBH_DP	N24	-	I/O	-	-	N/A	Diff. data positive

USBH_DM	N25	-	I/O	-	-	N/A	Diff. data negative
USB Device							
USBOTG_VBUS	U22	GPIO5_25	I	PD 100K	5V	N/A	VBUS detection
USBOTG_DP	P24	-	I/O	-	3,0V	N/A	Diff. data positive
USBOTG_DM	P25	-	I/O	-	3,0V	N/A	Diff. data negative
UART							
UART-A_TXD	A3	GPIO0_9	O	PU 10K	3,3V	8mA	UART transmit data
UART-A_RXD	C4	GPIO0_8	I	IPU	3,3V	N/A	UART receive data
UART-A_RTS	A2	GPIO0_12	O	IPU	3,3V	8mA	UART modem control
UART-A_CTS	B3	GPIO0_11	I	IPU	3,3V	N/A	UART modem control
UART-C_TXD	A4	GPIO0_4	O	PU 10K	3,3V	8mA	UART transmit data
UART-C_RXD	C6	GPIO0_3	I	IPU	3,3V	N/A	UART receive data
UART-D_TXD	D2	GPIO1_15	O	PU 10K	3,3V	8mA	UART transmit data
UART-D_RXD	D1	GPIO1_14	I	IPU	3,3V	N/A	UART receive data
CAN							
CAN1_TX	AE17	GPIO2-17	O	IPU	3,3V	8mA	transmit data
CAN1_RX	AC14	GPIO2-16	I	PU 10K	3,3V	N/A	receive data
CAN2_TX	AD5	GPIO5-6	O	IPU	3,3V	8mA	transmit data
CAN2_RX	AB6	GPIO5-5	I	PU 10K	3,3V	N/A	receive data
LCD (RGB Display)							
LCD_PIXCLK	AE14	GPIO2_25	O	SR 22R	3,3V	8mA	LCD data clock
LCD_DISP	AE18	GPIO2_30	O		3,3V	8mA	LCD data enable signal
LCD_VSYNC	AB14	GPIO2_28	O		3,3V	8mA	LCD frame sync
LCD_HSYNC	AD13	GPIO2_27	O		3,3V	8mA	LCD line sync

LCD_D0	AA15	GPIO2_18	O		3,3V	8mA	LCD B2
LCD_D1	AB15	GPIO2_19	O		3,3V	8mA	LCD B3
LCD_D2	AD14	GPIO2-20	O		3,3V	8mA	LCD B4
LCD_D3	AD15	GPIO2-21	O		3,3V	8mA	LCD B5
LCD_D4	AA14	GPIO2-22	O		3,3V	8mA	LCD B6
LCD_D5	AC15	GPIO2-23	O		3,3V	8mA	LCD B7
LCD_D6	AD18	GPIO2-10	O		3,3V	8mA	LCD G2
LCD_D7	AD16	GPIO2-11	O		3,3V	8mA	LCD G3
LCD_D8	AB17	GPIO2-12	O		3,3V	8mA	LCD G4
LCD_D9	AA16	GPIO2-13	O		3,3V	8mA	LCD G5
LCD_D10	AE16	GPIO2-14	O		3,3V	8mA	LCD G6
LCD_D11	AC16	GPIO2-15	O		3,3V	8mA	LCD G7
LCD_D12	AE19	GPIO2-2	O		3,3V	8mA	LCD R2
LCD_D13	AC18	GPIO2-3	O		3,3V	8mA	LCD R3
LCD_D14	AD19	GPIO2-4	O		3,3V	8mA	LCD R4
LCD_D15	AD17	GPIO2-5	O		3,3V	8mA	LCD R5
LCD_D16	AC17	GPIO2-6	O		3,3V	8mA	LCD R6
LCD_D17	AC19	GPIO2-7	O		3,3V	8mA	LCD R7
LCD_PANEL_EN	L5	GPIO1-24	O		3,3V	4mA	LCD panel power enable
LCD_BL_EN	C2	GPIO1-23	O		3,3V	4mA	LCD backlight power enable
LCD_BL_CTRL	F2	GPIO0-21	O		3,3V	8mA	LCD backlight brightness control (PWM4)
LVDS 1							
LVDS1_CLK_P	-	-	A I/O	-	-	N/A	P signal of diff. LVDS clock
LVDS1_CLK_N	-	-	A I/O	-	-	N/A	N signal of diff. LVDS clock
LVDS1_TX0_P	-	-	A I/O	-	-	N/A	P signal of diff. LVDS data
LVDS1_TX0_N	-	-	A I/O	-	-	N/A	N signal of diff. LVDS data
LVDS1_TX1_P	-	-	A I/O	-	-	N/A	P signal of diff. LVDS data
LVDS1_TX1_N	-	-	A I/O	-	-	N/A	N signal of diff. LVDS data
LVDS1_TX2_P	-	-	A I/O	-	-	N/A	P signal of diff. LVDS data
LVDS1_TX2_N	-	-	A I/O	-	-	N/A	N signal of diff. LVDS data

LVDS1_TX3_P	-	-	A I/O	-	-	N/A	P signal of diff. LVDS data
LVDS1_TX3_N	-	-	A I/O	-	-	N/A	N signal of diff. LVDS data
LVDS1_PANEL_EN	H3	GPIO0-27	O	IPU	3,3V	8mA	LVDS panel power enable
LVDS1_BL_EN	G5	GPIO0-22	O	IPU	3,3V	8mA	LVDS backlight power enable
LVDS1_BL_CTRL	D5	GPIO0-13	O	IPU	3,3V	8mA	LVDS backlight brightness control (PWM2)
CPI1 Camera Input							
CPI1_D0	AB5	GPIO5-12	I	IPU	3,3V	N/A	Video image input data
CPI1_D1	AC5	GPIO5-13	I	IPU	3,3V	N/A	Video image input data
CPI1_D2	AE4	GPIO5-14	I	IPU	3,3V	N/A	Video image input data
CPI1_D3	AD4	GPIO5-15	I	IPU	3,3V	N/A	Video image input data
CPI1_D4	AC4	GPIO5-16	I	IPU	3,3V	N/A	Video image input data
CPI1_D5	AE3	GPIO5-17	I	IPU	3,3V	N/A	Video image input data
CPI2_D6	AD3	GPIO5-18	I	IPU	3,3V	N/A	Video image input data
CPI1_D7	AD2	GPIO5-19	I	IPU	3,3V	N/A	Video image input data
CPI1_PIXCLK	AE6	GPIO5-11	I	IPU	3,3V	N/A	Video clock input
CPI1_HSYNC	AC1	GPIO5-22	I	IPU	3,3V	N/A	Video hsync input
CPI1_VSYNC	AC2	GPIO5-23	I	IPU	3,3V	N/A	Video vsync input
SD Card Interface 1							
SDC1_D0	AC11	GPIO6-2	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC1_D1	AD11	GPIO6-3	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC1_D2	AE11	GPIO6-4	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC1_D3	AA12	GPIO6-5	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC1_CMD	AD12	GPIO6-1	I/O	PU 10K	1,8V/3,3V	16mA	CMD signal
SDC1_CLK	AE12	GPIO6-0	O	SR 22R	1,8V/3,3V	16mA	SDC Clock output
SDC1_CD#	AB12	GPIO6-6	I	PU 10K	1,8V/3,3V	16mA	Card detect input
SDC1_WP	AA13	GPIO6-7	I	PU 10K	1,8V/3,3V	16mA	Write protect input
SD Card Interface 2							
SDC2_D0	AD7	GPIO6-10	I/O	PU 10K	1,8V/3,3V	16mA	SDC data

SDC2_D1	AE7	GPIO6-11	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC2_D2	AB8	GPIO6-12	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC2_D3	AC8	GPIO6-13	I/O	PU 10K	1,8V/3,3V	16mA	SDC data
SDC2_CMD	AA8	GPIO6-9	I/O	PU 10K	1,8V/3,3V	16mA	CMD signal
SDC2_CLK	AE8	GPIO6-8	O	SR 22R	1,8V/3,3V	16mA	SDC Clock output
SDC2_CD#	AD8	GPIO6-14	I	PU 10K	1,8V/3,3V	16mA	Card detect input
SDC2_WP	AE9	GPIO6-15	I	PU 10K	1,8V/3,3V	16mA	Write protect input
SPI1							
SPI1_CS0#	G3	GPIO0-28	O	PU 10K	3,3V	8mA	SPI slave select
SPI1_SCK	J4	GPIO0-26	O	-	3,3V	8mA	SPI clock
SPI1_MISO	J5	GPIO0-24	I	IPU	3,3V	N/A	SPI data from slave
SPI1_MOSI	G2	GPIO0-25	O	IPU	3,3V	8mA	SPI data to slave
SPI2							
SPI2_CS0#	H2	GPIO1-2	O	PU 10K	3,3V	8mA	SPI slave select
SPI2_SCK	J2	GPIO1-0	O	-	3,3V	8mA	SPI clock
SPI2_MISO	K5	GPIO0-30	I	IPU	3,3V	N/A	SPI data from slave
SPI2_MOSI	H1	GPIO0-31	O	IPU	3,3V	8mA	SPI data to slave
I2C1							
I2C1_SCL	AA18	GPIO2-0	I/O	PU 2K2	3,3V	8mA	I^2C clock
I2C1_SDA	AB18	GPIO2-1	I/O	PU 2K2	3,3V	8mA	I^2C data
I2C2							
I2C2_SCL	AA17	GPIO2-8	I/O	PU 2K2	3,3V	8mA	I^2C clock
I2C2_SDA	AB16	GPIO2-9	I/O	PU 2K2	3,3V	8mA	I^2C data
Audio SSI							
AUDIO_RXD	Y21	GPIO5-9	I		3,3V	N/A	Audio input data
AUDIO_TXD	AA6	GPIO5-3	O		3,3V	8mA	Audio output data

AUDIO_TXC	AE5	GPIO5-1	I/O		3,3V	8mA	Audio transmit bit clock
AUDIO_TXFS	AA7	GPIO5-2	I/O		3,3V	8mA	Audio transmit frame select
AUDIO_RXC	AD22	GPIO5-7	I/O		3,3V	8mA	Audio transmit bit clock
AUDIO_TXFS	AB21	GPIO5-8	I/O		3,3V	8mA	Audio transmit frame select
AUDIO_MCLK	AB7	GPIO5-0	I		3,3V	N/A	Audio master clock
GPIO							
GPIO1	E6	GPIO0-1	I/O		3,3V	8mA	digital input / output
GPIO2	A5	GPIO0-2	I/O		3,3V	8mA	digital input / output
GPIO3	AD6	GPIO5-4	I/O		3,3V	8mA	digital input / output
GPIO4	AA19	GPIO4-31	I/O		3,3V	8mA	digital input / output
GPIO5	AA20	GPIO4-26	I/O		3,3V	8mA	digital input / output
GPIO6	AE21	GPIO4-29	I/O		3,3V	8mA	digital input / output
Manufacturing							
JTAG_TCK	N22	-	I	PU 4K7	1,8V	N/A	JTAG clock input (JTAG_TCK and JTAG_RTCK are shorted)
JTAG_TMS	P21	-	I	PU 4K7	1,8V	N/A	JTAG mode select
JTAG_TRST#	N21	-	I	PD 1K	1,8V	N/A	JTAG reset
JTAG_TDI	R22	-	I	PU 4K7	1,8V	N/A	JTAG Data input
JTAG_TDO	P22	-	O		1,8V	4mA	JTAG Data output
JTAG_RTCK	N22	-	O	PU 4K7	1,8V	N/A	JTAG return TCK (JTAG_TCK and JTAG_RTCK are shorted)
JTAG_MOD	M2	GPIO1-25	I	PU 10K	3,3V	N/A	Mode selection JTAG/Boundary Scan
JTAG_RESET#			I	PU 10K	1,8V	N/A	JTAG reset
JTAG_VCC			O		1,8V		VCC reference
Miscellaneous							
IRQ_1	R23		I	PD 12K	3,3V	N/A	Interrupt input
IRQ_TOUCH1#	D6	GPIO0-0	I	PU 10K	3,3V	N/A	Interrupt input for touch controller
IRQ_TOUCH2#	B5	GPIO0-7	I	PU 10K	3,3V	N/A	Interrupt input for touch controller

POWERFAIL#	Y4	GPIO3-31	I	PU 10K	3,3V	N/A	Power Fail
PWM_FAN	E4	GPIO0-10	O		3,3V	8mA	PWM signal for fan control (PWM5)
RESI#			I	PU 10K	3,3V	N/A	Reset input from carrier board
RESO#			O	-	3,3V	16mA	Reset output to carrier board
POWER_ON_BASE			O	-	3,3V	20mA	Power enable signal for the 3.3V baseboard supply
SUSPEND#			O	-	3,3V	20mA	Power switching signal for VCC_5V
ON_OFF#			I	PU 100K	2,5V	N/A	Power management signal
Power Supply							
BAT			-	-	2,3V–3,3V	N/A	Battery backup input for RTC
VCC_5V			-	-	-	N/A	+ 5V supply
VCC_STANDBY			-	-	-	N/A	+ 5V standby supply
GND			-	-	-	N/A	Ground

8 Technical Characteristics

8.1 Electrical Specifications

Supply voltage	5V, +/-5%
Current consumption	up to 1.6 A

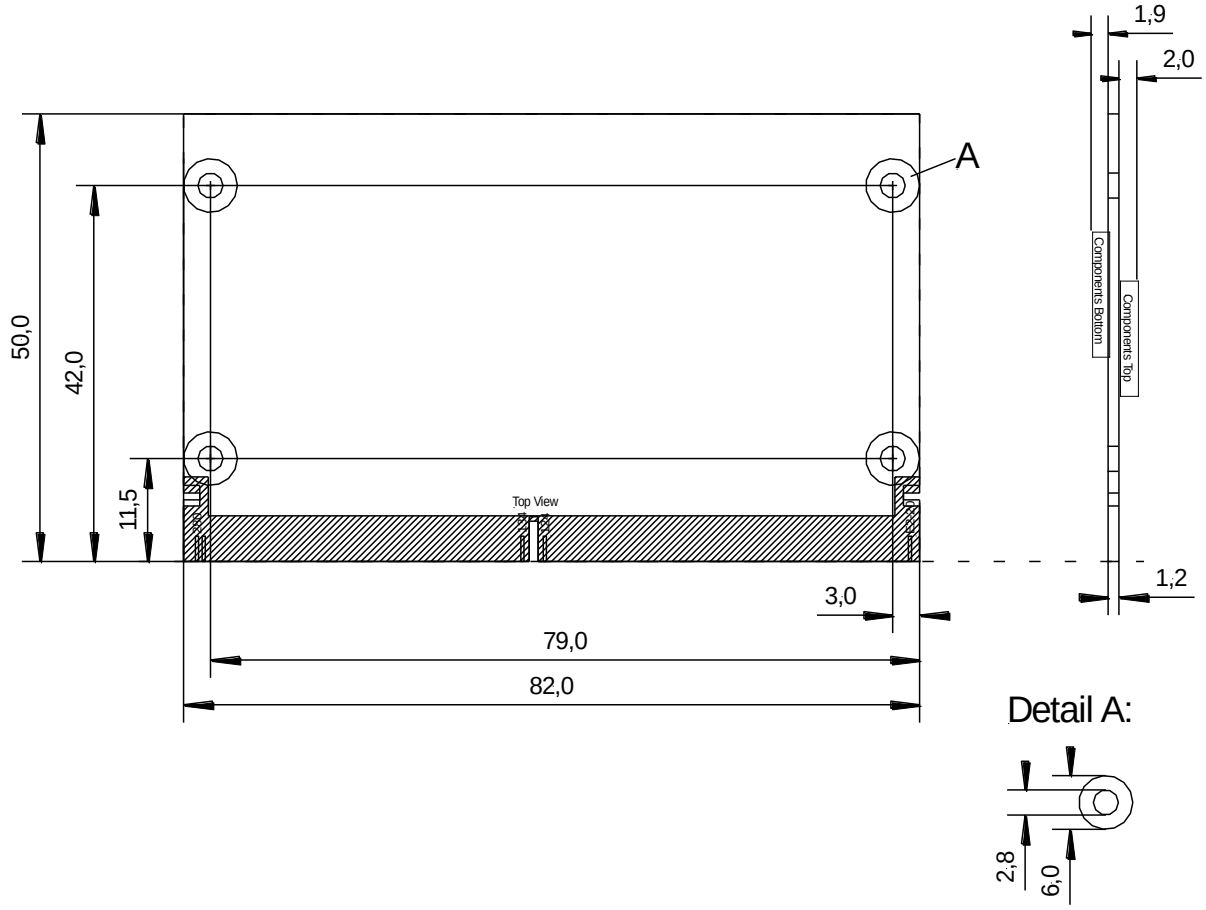
8.2 Environmental Specifications

Operating temperature Standard: Extended: **Storage temperature**	 0 ... +70°C -40 ... +85°C -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

8.3 Mechanical Specifications

Weight	approx. 19 g
Board	FR-4, UL-listed, 10 layers
Dimensions	82.2 mm x 50.0 mm x 5.0 mm

9 Dimensional Drawing



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