DIMM.AM335x

Hardware Manual

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emtrion GmbH

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Rev	Date/Signature	Changes
1	24.08.2012/Bue	First revision
2	25.10.2012/Bue	In chapter 4.1 signal 3V3_ON at pin 135 of the SODIMM connector renamed to POWER_ON_BASE to conform to other documents. In chapter 5.1 signal POWER_ON_BASE added.
3	16.12.2014/Bue	In chapter 3.18 temperature characteristics of RTC added. Picture at first page replaced by picture of rev 2 board. Bookmarks added .

Content

1 Introduction

The DIMM-AM335x processor module is a SODIMM sized CPU board based on the processor AM3352ZCZD72 or AM3354ZCZD72 from Texas Instruments.

The AM3352ZCZD72 is based on an ARM® Cortex-A8 core running at up to 720 MHz (Turbo Mode). It includes a variety of functions required industrial communication applications. Besides a variety of serial communication interfaces also interfaces for display, mass storage devices and memory devices are integrated in the processor.

The CPU is accompanied by up to 512 MB DDR3 SDRAM, 8 MB NOR flash and up to 8 GB SLC NAND flash. Also an integrated power management controller is added.

All interfaces are accessible through a 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2.5V keying.

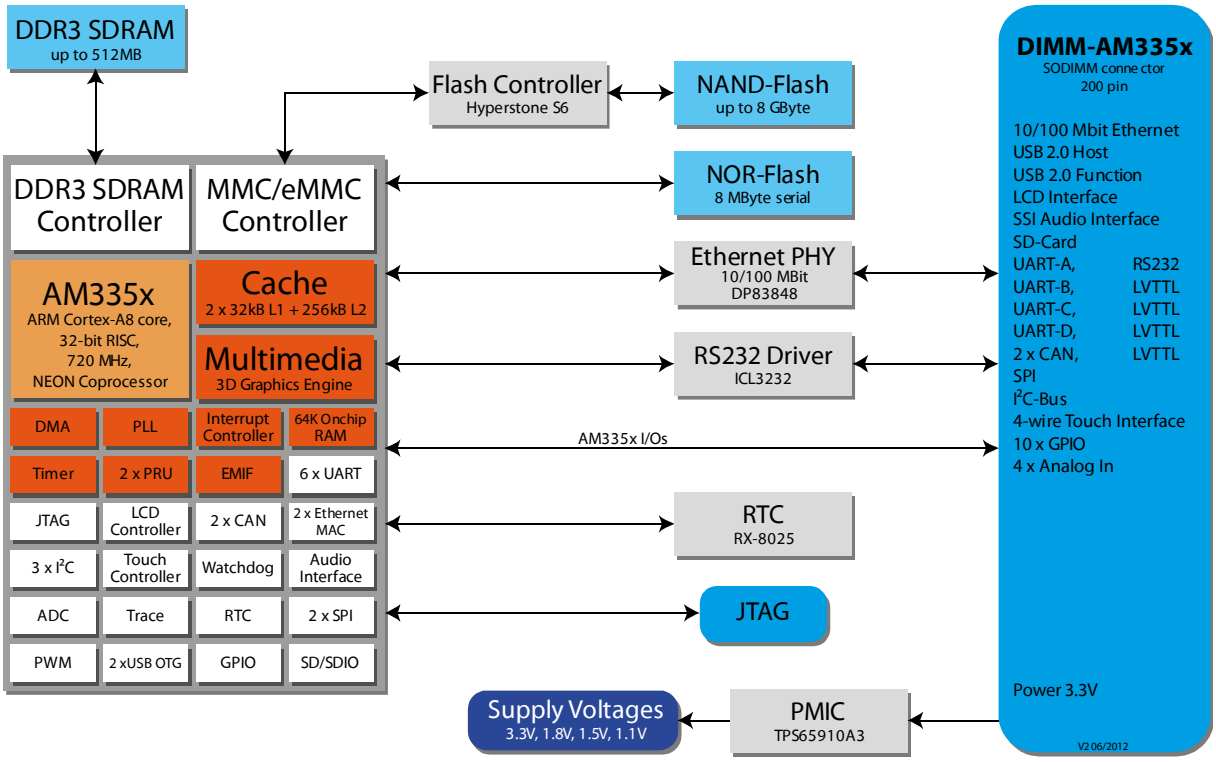
The following table summarizes the main features and interfaces of the DIMM-AM335x module:

DIMM-AM335x
CPU AM3352 or AM3354
up to 512 MB DDR3 SDRAM
8 MB NOR Flash
up to 8 GB SLC NAND Flash
10/100Mbit Ethernet
USB 2.0 Host
USB 2.0 OTG
LCD Interface max WXGA, 24bpp (1280 x 765)
4 wire resistive Touch
IIS Audio Interface
1 x UART RS232
4 x UART LVTTL
2 x CAN V2.0B
SD Card interface
SPI
I^2C
10 x digital IO, 4 x analog In
RTC
JTAG interface
3.3V supply
Operating temperature range -20°C to 85°C

The CPU AM3354 distinguishes itself from the AM3352 by an additionally incorporated Graphics Engine SGX530 to accelerate 3D graphic display.

2 Block Diagram

The following figure shows the block diagram of the DIMM-AM335x.



3 Functional Description

3.1 Processor AM335x

The DIMM-AM335x module is either based on the CPU AM3352 or AM3354from Texas Instruments. It utilizes an ARM® Cortex-A8 core running at up to 720 MHz. Compared to the AM3352 the CPU AM3354 includes an additional SGX530 3D graphics accelerator function block.

In addition to the CPU core with MMU, FPU and Cache, the processor provides the following memory interfaces and peripheral function blocks:

- LCD interface up to 1280 x 768 pixels with up to 24 bpp colour depth
- DDR2/3 SDRAM controller
- Memory card interfaces, 2 x SDC/SDIO
- 2 x USB 2.0 OTG
- Serial interfaces including 4 x UART, I^2C, SPI, IIS
- DMA controller
- Interrupt controller
- 15 channel interval timer
- Various GPIOs
- Power management
- Internal memories: 128 kB SRAM and 64 kB ROM containing bootloader
- JTAG debug interface

Watch:

- The processor bus interface is not available since the pins are multiplexed with pins of the LCD and MMC interfaces

Further details of the processor can be found in the AM335x documents from Texas Instruments [1].

3.1.1 Processor Clocks

All clocks needed for the different peripheral functions of the processor are derived from a 24 MHz crystal which used as master clock input. The processor is normally operated in Turbo mode. This means:

- CPU clock 720 MHz
- DDR3 clock 303 MHz
- L3 clock 200 MHz
- L4 clock 100 MHz ($^1/_2$ * L3 clock)

Additionally a 32.768 kHz clock is supplied for the integrated RTC and power down operating modes of the CPU.

3.1.2 Boot Mode

The processor AM335x has an integrated Boot ROM which supports 31 different boot configurations. Each configuration consists of a sequence of 4 different boot devices that are checked in series for valid boot data. The configuration is selected by the five configuration pins SYSBOOT[4:0].

The following sequences are preferred:

- SPI0 – MMC0 – UART0 – EMAC1 0x16
- EMAC1 –SPI0 – NAND – NANDI2C 0x06

In normal operation a serial NOR flash which is connected to SPI0 is used as primary boot device. For development and production purposes EMAC1 can be selected as primary boot medium

The boot sequence is selected via the two DIP Switches SW1-2 and SW1-1:

SW1-2	SW1-1	1st Boot device
off	**off**	SPI0
off	**on**	EMAC1
on	**off**	USB0
on	**on**	UART0

Watch: Booting from the eMMC/NAND connected to the MMC1 interface is not possible!

3.1.3 Interrupts

The processor AM335x incorporates an integrated interrupt controller. It processes incoming interrupts by masking and priority sorting to produce the interrupt signals for the CPU.

4 GPIO pins are used to cause unique interrupt requests for the PMIC and 3 external devices connected at the SODIMM connector.

AM335x GPIO	Source
GPIO1_16	PMIC
GPIO0_6	SODIMM NMI
GPIO2_26	SODIMM IRQ-A
GPIO3_0	SODIMM IRQ-B

The signalling level of all interrupts is 3.3V. The interrupts can be programmed to be edge or level sensitive.

3.2 NOR-Flash

An 8 MByte serial NOR flash of type MX25L6445M2I-10G von Macronix is used as primary boot device. It is connected to the interface SPI0.

The integrated bootloader of the processor supports booting from the NOR flash. Booting from NOR Flash is enabled if DIP switch SW1-1 is off.

Hardware write protection of the NOR flash is realized by the port pin GPIO3_4 of the processor. A low level protects the flash device. During and after Reset the pin is driven low by the processor. Besides the hardware protection the chip also supports a software protection.

Watch:

The processor operates in little-endian mode while the serial NOR flash operates in big-endian mode (MSB first). The image data must be stored in the flash in big-endian format because the processor does not convert the endianess of the data.

3.3 NAND Flash

The NAND Flash interface of the board is built from a flash controller S6 from Hyperstone and an SLC NAND flash chip.

The S6 is connected to the MMC1 interface of the processor. It behaves as an SD Card that conforms to SD Physical Layer specification 3.0. NAND Flash chips from various manufacturers with up to 8 GByte capacity can be connected.

The standard flash capacity is 256 MByte.

3.4 DDR SDRAM

256 MByte or 512 MByte DDR3 SDRAM are soldered.

The RAM is clocked with 303 MHz and accessed with CAS latency 5. The data bus is 16 bit wide.

The RAM is located in the address range 0x8000_0000 … 0xBFFF_FFFF. The address range spans 1 GB. Smaller memories are mirrored within that range.

3.5 Processor Bus Interface

The processor bus interface is not available at the SODIMM connector since most of the pins are multiplexed with pins of peripheral functions.

3.6 Ethernet

Two 100Base-TX Ethernet interfaces are incorporated in the CPU AM335x. Because of the pin multiplexing only RMII1 interface is available.

An Ethernet PHY DP83848K from Texas Instruments is used. The PHY address is 1. A 50 MHz oscillator is used as reference clock of the RMII interface.

The Ethernet signal line pairs ETH_TDP/ETH_TDM and ETH_RDP/ETH_RDM as well as two status signals SPEED_LED# and LINK_LED# are connected to the SODIMM connector.

The signal LINK_LED# indicates if data packages are transferred. If a link is established every packet causes an 80 ms long low pulse.

The signal SPEED_LED# indicates the transfer speed of the connection. Low = 100 Mbit/s, high = 10 Mbit/s.

A 1:1 transformer with center taps connected to 3.3V, must be added externally to the signal lines.

3.7 USB Interfaces

Two USB Rev 2.0 OTG compliant controllers are integrated in the processor AM335x. High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) transfers are supported. Each controller has a 32 kByte Endpoint FIFO for transmit and receive.

At the SODIMM connector pins for one host and one device interface are provided.

The controller USB0 is always operated as a Host interface. The power switch control output USBH_PEN# is part of the USB controller. The overcurrent signal input USBH_OC# from the SODIMM connector is connected to GPIO pin GPIO1_20 of the processor. A logical “0” signals overcurrent.

The second controller, USB1, is used in OTG mode. The ID input is pulled high on the module by a 10 KΩ resistor which preconfigures it to operate in device mode. For that operating mode the VBUS input is available at the SODIMM pin USBF_VBUS. Now power is drawn from that pin. It is only used to signal that a Host is connected.

Additionally the ID input can be controlled by the signal USB1_ID at the SODIMM connector. Thus the mode can be switched between Device and Host mode by an external source. In the Host mode the VBUS power switch control output USB1_PEN# is controlled by the USB controller and available at pin 131 of the SODIMM connector. The corresponding overcurrent signal input USB1_OC# from the SODIMM connector is connected with GPIO pin GPIO1_21of the processor. A logical “0” signals overcurrent.

All necessary termination resistors are incorporated in the processor. No external resistors are needed.

3.8 LCD Interface

3.8.1 General

The processor AM335x incorporates an LCD controller that can drive displays with resolutions up to 1280 x 768 pixels (WXGA). The colour depth is fixed at 24 bpp (RGB888).

The pixel clock is generated internally. Sourcing an external LCD clock is not possible.

All data and control lines are available at the SODIMM connector.

3.8.2 LCD interface

The following table describes the function of the data and control lines in RGB mode.

Signal	Description
LCD_D[23:0]	Colour data, mapping according to the following table
LCD_VSYNC	Vertical synchronization signal
LCD_HSYNC	Horizontal synchronization signal
LCD_DISP	Data enable signal signaling active data
LCD_DCK	Pixel clock

The following table shows the RGB colour mapping of the LCD_D[23:0] pins at the SODIMM connector:

LCD_D[23:0]	RGB888 (24bit)
LCD_D0	B2
LCD_D1	B3
LCD_D2	B4
LCD_D3	B5
LCD_D4	B6
LCD_D5	B7
LCD_D6	G2
LCD_D7	G3
LCD_D8	G4
LCD_D9	G5
LCD_D10	G6
LCD_D11	G7
LCD_D12	R2
LCD_D13	R3
LCD_D14	R4
LCD_D15	R5
LCD_D16	R6
LCD_D17	R7
LCD_D18	R1
LCD_D19	G1
LCD_D20	B1
LCD_D21	R0
LCD_D22	G0
LCD_D23	B0

Watch:

The colour mapping of the SODIMM connector fits to emtrion's carrier boards Lothron and Verno if the LCD Controller is operated in RGB888 mode. Only the lower 18 bits are used at the display connector of the carrier boards.

3 additional GPIO output signals are provided to control the power supply of the display and the backlight.

Signal	Description
LCD_VEPWC	Optional display power control output, driven by GPIO1_29
LCD_VCPWC	Optional display power control output, driven by GPIO2_27
LCD_DON	Display power enable signal, driven by GPIO2_2 Signal is used to switch the backlight power (“0” backlight off; “1” backlight on)

3.9 Touch Interface

A 4-wire resistive touch screen controller is incorporated in the processor AM335x.

The 4 touch interface signals TOUCH_XP, TOUCH_XM, TOUCH_YP and TOUCH_YM are available at the SODIMM connector.

3.10 Audio Interface

The serial interface MCASP1 of the processor AM335x is available as I2S audio interface at the SODIMM connector to connect an external audio codec.

The interface can be operated in master or slave mode. Different clocks for receive and transmit are possible.

3.11 CAN Controller

Two CAN interfaces are incorporated in the processor AM335x. Both interfaces support CAN specification V2.0B with up to 1Maud transfer rate. The message RAMs can store 64 message objects.

The receive line and the transmit line of the controller CAN0 are available at the specified pins of the SODIMM connector. The signals have LVTTL level and an appropriate CAN transceiver must be added externally.

The signal lines of the second CAN controller CAN1 are optionally available at the pins RTS and CTS of UART3.

3.12 SDC/SDIO Interface

The processor AM335x incorporates 3 SDC/SDIO interfaces which are compatible to the SD Physical Layer specification 3.0. All interfaces have 8 data lines and provide inputs for card detect and write protect status.

The interface MMC0 is unavailable because of pin multiplexing.

The interface MMC1 is used onboard to connect the NAND flash. All 8 data lines are used for the flash interface.

The control signals and the lower 4 data lines of interface MMC2 are routed to the SDC1 interface of the SODIMM connector. Since the interface SDC2 of the SODIMM connector is unused the upper 4 data lines of the MMC2 interface are routed its data pins.

An SDC socket with 4 data pins can be directly connected at the SDC1 interface. If an interface like MMCplus with 8 data lines shall be realized the upper 4 data bits can be taken from the SDC2 interface.

The write protect input SDC1_WP of the SDC interface is connected to GPIO pin GPIO1_26 of the processor. The card detect input SDC1_CD# is connected to GPIO pin GPIO1_27 of the processor.

3.13 Serial Ports

The processor AM335x incorporates 6 TL16C750 compatible UARTs. The TL16C750 has 64 Byte FIFOs. The baud rates are generated internally by dividing a 48 MHz input clock.

The signals of 4 UARTs are available at the SODIMM connector.

UART0 is used as terminal interface and the signals are connected by an RS232 transceiver like MAX3221E is to UART0 on the DIMM module.

The signals of UART1, UART3 and UART4 are connected directly as LVTTL signals to the SODIMM connector. The modem control signals RTS and CTS of UART3 are connected to the pins of UARTE. UART1 provides all 6 modem control signals. They are routed to the GPIO[9:4] pins of the SODIMM connector.

SODIMM interface	AM335x interface	Signal level
UART_A	UART0, TxD, RxD, RTS and CTS	RS232
UART_B	UART1, with all modem control signals at GPIO[9:4]	LVTTL
UART_C	UART4, TxD and RxD	LVTTL
UART_D	UART3, TxD and RxD	LVTTL
UART_E	UART3, RTS and CTS	LVTTL

3.14 I^2C- Bus

The I^2C bus interface I2C0 of the processor AM335x is used on the module DIMM-335x. It supports baud rates from 100 Kbits/s up to 3.4 Mb/s. 32 byte FIFOs are incorporated to buffer transmit and receive telegrams.

The PMIC TPS65910A3 and the RTC RX-8025 are connected to the I^2C bus on the module. The PMIC uses the two 7-bit addresses, 0x2D and 0x12. The RTC uses the address 0x32.

The I^2C bus is available at the SODIMM connector for external devices. The SCL and SDA lines are pulled up to 3.3V with 2.2 kΩ resistors.

3.15 SPI Interface

The SPI1 interface of the AM335x is available at the SODIMM connector. The characteristics of the interface can be individually controlled by software.

3.16 Digital and Analog I/Os

10 digital GPIO pins are provided normally at the SODIMM connector. All but 2 pins of the DIMM.AM335x module can be used as simple GPIOs or can be programmed with their special function.

The pins have the following characteristics:

SODIMM Pin	GPIO	Special Function
GPIO_0	GPIO0_7	PWM0
GPIO_1	- ***	USB1_ID
GPIO_2	GPIO1_21	USB1_OC#
GPIO_3	- ***	USB1_PEN#
GPIO_4	GPIO2_19	UART1_RI
GPIO_5	GPIO3_9	UART1_DCD
GPIO_6	GPIO2_18	UART1_DTR
GPIO_7	GPIO3_10	UART1_DSR
GPIO_8	GPIO0_13	UART1_RTS
GPIO_9	GPIO0_12	UART1_CTS

*** no GPIO function available

Besides the digital I/Os 4 analogue inputs of the AM335x are available at the SODIMM connector:

SODIMM Pin	Signal
ANA_IN1	AIN4
ANA_IN2	AIN5
ANA_IN3	AIN6
ANA_IN4	AIN7

The analogue inputs are controlled by the touch controller. In mixed mode they can be used as general purpose inputs in parallel to the 4-wire touch screen inputs. Triggering of the conversions must be done by software.

The integrated ADC has 12-bit resolution. The minimum conversion time is 15 ADC clock cycles. Input voltages must not exceed 3.3 V.

3.17 Status LED

A bicolour LED is located on the top side of the DIMM-AM335x module. This LED is normally used to signal the health state of the software.

After reset the LED shines red. After the bootloader has successfully started the LED shines green.

The LED is controlled by the two GPIO pins of the AM335x. Pin GPIO2_4 drives the green LED, pin GPIO2_5 drives the red LED. Watch that the green LED is active low while the red LED is active high. This gives the following colour table:

LED	GPIO2_4	GPIO2_5
green	0	0
yellow	0	1
off	1	0
red	1	1

3.18 RTC

The current consumption of the integrated RTC of the CPU is too high to be buffered by a battery. Therefore an external RTC RX-8025 from Epson is added. This RTC has a current consumption of about 0.5 µA and is buffered by an external battery connected to the BAT pin of the SODIMM connector.

While the board is powered the 32 kHz clock of the RTC is connected to the CPU. Therefore the time information can be copied at power on from the Epson RTC to the integrated RTC of the processor and both count with the same clock source.

The RTC RX-8025 is connected to the I^2C interface and uses the 7 bit address 0x32.

The frequency precision of the RTC is given with 5 +/-5 ppm at 25°C and a maximum deviation of +10 / -120ppm over the temperature range -20°C …+70°C.

3.19 Reset

There are several ways to reset the board:

- The PMIC supervises all voltages and causes a power on reset in undervoltage situations
- A low pulse at pin RESI# of the SODIMM connector causes a power on reset
- Setting the PRM_RSTCTRL.RST_GLOBAL_COLD_SW bit in the PRM memory map causes a power on reset. This bit is self-clearing; it is automatically cleared by the hardware.
- A low signal at pin CSRSTZ# of the Debug connector causes a warm reset

All resets also reset the Ethernet PHY and the Flash interface. Also the reset signal is driven to the pin RESO# at the SODIMM connector to reset external devices.

3.20 Power Supply, PMIC

The maximum power consumption of the module DIMM-AM335x is 0.6 A at +3.3 V, +/- 5%. This voltage must be supplied via the SODIMM connector. All further voltages needed are generated on board by the power management controller (PMIC) TPS65910A3 from Texas Instruments [2].

The PMIC generates all voltages and cares about the appropriate voltage sequencing at power up and down. The voltages can be controlled by the processor AM335x via an I^2C interface. The PMIC incorporates two interfaces with the 7-bit I^2C addresses 0x12 and 0x2D.

4 Connectors

4.1 J1, SODIMM

Type 200 pin SODIMM edge connector, 2.5V keying

Pin	Signal	Interface		Signal	Pin
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2
3	ETH_TDP			USBH_OC#	4
5	ETH_TDM			USBH_DM	6
7	GND			USBH_DP	8
9	ETH_RDP		USB Device	USBF_VBUS	10
11	ETH_RDM			USBF_DM	12
13	LINK_LED#			USBF_DP	14
15	USBH_VBUS	USB Host	Power	GND	16
17	CAN0_TX	CAN	UART-A	UART0_TXD#	18
19	CAN0_RX			UART0_RXD#	20
21	UART3_RTS/CAN1_RX	UART-E		UART0_RTS#	22
23	UART3_CTS/CAN1_TX			UART0_CTS#	24
25	UART3_TXD	UART-D	Touch	Touch_XP	26
27	UART3_RXD			Touch_XM	28
29	UART4_TXD	UART-C		Touch_YP	30
31	UART4_RXD			Touch_YM	32
33	UART1_TXD	UART-B	A/D	ANA_IN1	34
35	UART1_RXD			ANA_IN2	36
37	ANA_IN4	A/D		ANA_IN3	38
39	+3V3	Power		GND	40
41	LCD_D22	LCD		LCD_D23	42
43	LCD_D20			LCD_D21	44
45	LCD_D18			LCD_D19	46
47	LCD_D16			LCD_D17	48
49	LCD_D14			LCD_D15	50
51	LCD_D12			LCD_D13	52
53	LCD_D10			LCD_D11	54
55	LCD_D8			LCD_D9	56
57	LCD_D6			LCD_D7	58
59	LCD_D4			LCD_D5	60
61	LCD_D2			LCD_D3	62
63	LCD_D0			LCD_D1	64
65	+3V3	Power		GND	66

67	n/c	**LCD**		n/c	**68**
69	LCD_DISP			LCD_DCK	**70**
71	LCD_HSYN			LCD_DON	**72**
73	LCD_VSYN			LCD_VCPWC	**74**
75	n/c			LCD_VEPWC	**76**
77	n/c	**VIO, VOU**		n/c	**78**
79	n/c			n/c	**80**
81	n/c			n/c	**82**
83	n/c			n/c	**84**
85	n/c			n/c	**86**
87	n/c			n/c	**88**
89	n/c			n/c – SPI_SEL2	**90**
91	n/c			n/c – SPI_SEL1	**92**
93	+3V3	**Power**		GND	**94**
95	SDC2_D4	**SDC**	**SDC/SDIO**	SDC2_D0	**96**
97	SDC2_D5			SDC2_D1	**98**
99	SDC2_D6			SDC2_D2	**100**
101	SDC2_D7			SDC2_D3	**102**
103	n/c			SDC2_CMD	**104**
105	n/c			SDC2_CLK	**106**
107	n/c			SDC2_CD#	**108**
109	n/c			SDC2_WP	**110**
111	SPI1_SS0#	**SPI**		SPI1_MISO	**112**
113	SPI1_SCK			SPI1_MOSI	**114**
115	SCL	**I2C**	**Audio**	AUDIO_BCK	**116**
117	SDA			AUDIO_LRC	**118**
119	n/c	**SPDIF**		AUDIO_DATI	**120**
121	GND			AUDIO_DATO	**122**
123	GND	**Power**		n/c	**124**
125	GPIO8/UART1_RTS	**GPIO**		GPIO9/UART1_CTS#	**126**
127	GPIO6/UART1_DTR#			GPIO7/UART1_DSR#	**128**
129	GPIO4/UART1_RI#			GPIO5/UART1_DCD#	**130**
131	GPIO2/USB1_OC#			GPIO3/USB1_PEN#	**132**
133	GPIO0/PWM0			GPIO1/USB1_ID	**134**
135	POWER_ON_BASE	**PWR Control**	**Power**	GND	**136**
137	n/c	**Address A[23:0]**		n/c	**138**

139	n/c		n/c	**140**
141	n/c		n/c	**142**
143	n/c		n/c	**144**
145	n/c		n/c	**146**
147	n/c		n/c	**148**
149	n/c		n/c	**150**
151	n/c		n/c	**152**
153	n/c		n/c	**154**
155	n/c		n/c	**156**
157	n/c		n/c	**158**
159	GND		n/c	**160**
161	+3V3	**Power**	GND	**162**
163	n/c	**Data D[15:0]**	n/c	**164**
165	n/c		n/c	**166**
167	n/c		n/c	**168**
169	n/c		n/c	**170**
171	n/c		n/c	**172**
173	n/c		n/c	**174**
175	n/c		n/c	**176**
177	n/c		n/c	**178**
179	PU1K	**Bus Control**	n/c	**180**
181	PU1K		PU1K	**182**
183	PU1K		IRQ-A	**184**
185	PU1K		IRQ-B	**186**
187	PU1K		NMI	**188**
189	PU1K		RESO#	**190**
191	PU1K		RESI#	**192**
193	PU1K		PU1K	**194**
195	n/c		PU1K	**196**
197	PU1K		n/c	**198**
199	BAT	**Power**	GND	**200**

4.2 J2, Debug Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	n/c	**2**	TCK
3	GND	**4**	GND
5	+1V8	**6**	TRST#
7	+3V3	**8**	+3V3
9	n/c	**10**	TDO
11	CFG_SCL	**12**	JTAG_DE#
13	CFG_SDA	**14**	TMS
15	CFG_WP	**16**	TDI
17	GND	**18**	JTAG_SEL
19	JTAG_RESI#	**20**	JTAG_RESI#

5 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	input
O	totem pole output
OD	open drain output
I/O	bidirectional

PU xK	pull-up resistor, x KΩ
PD xK	pull-down resistor, x KΩ
SR xR	series resistor x Ω
IPD	processor internal pull-down resistor, typ. 50 KΩ

5.1 J1, SODIMM Connector

Name	GPIO	Direction	Termination	Level [V]	Description
SPEED_LED#		OD		3.3	Speed indicator, 0 = 100Mb
ETH_TDP		AO		-	Ethernet TX pos.
ETH_TDM		AO		-	Ethernet TX neg.
ETH_RDP		AI		-	Ethernet RX pos.
ETH_RDN		AI		-	Ethernet RX neg.
LINK_LED#		OD		3.3	Traffic indicator
USBH_PEN#		O		3.3	Power enable signal for VBUS switch
USBH_OC#	GPIO1_20	I	PU 10K	3.3	Overcurrent signal from VBUS switch
USBH_DP		I/O	IPD 15K	-	USB data pos.
USBH_DM		I/O	IPD 15K	-	USB data neg.
USBF_VBUS		I	PD 15.6 K	5	VBUS detection
USBF_DP		I/O		-	USB data pos.
USBF_DM		I/O		-	USB data neg.
UART0_TXD#		O		RS232	UART transmit data
UART0_RXD#		I		RS232	UART receive data
UART1_TXD		O	PU 10K	3.3	UART transmit data
UART1_RXD		I		3.3	UART receive data
UART4_TXD		O		3.3	UART transmit data
UART4_RXD		I		3.3	UART receive data
UART3_TXD		O		3.3	UART transmit data
UART3_RXD		I		3.3	UART receive data
UART3_RTS/ CAN1_RX		O/I		3.3	UART flow control, CAN receive data
UART3_CTS/ CAN1_TX		I/O		3.3	UART flow control, CAN transmit data
CAN_TX		O		3.3	CAN transmit data
CAN_RX		I	PU 10K	3.3	CAN receive data
TOUCH_XP		A I/O		3.3	X pos terminal
TOUCH_XM		A I/O		3.3	X neg terminal

Name	GPIO	Direction	Termination	Level [V]	Description
TOUCH_YP		A I/O		3.3	Y pos terminal
TOUCH_YM		A I/O		3.3	Y neg terminal
ANA_IN1		AI		3.3	Analog input
ANA_IN2		AI		3.3	Analog input
LCD_DON	GPIO2_2	O		3.3	LCD display enable signal
LCD_DCK		O		3.3	LCD data clock
LCD_DISP		O		3.3	LCD data enable signal
LCD_VSYNC		O		3.3	LCD frame sync signal
LCD_HSYNC		O		3.3	LCD line sync signal
LCD_D[23:0]		O		3.3	LCD colour data
LCD_VEPWC	GPIO1_29	O		3.3	Optional LCD power control
LCD_VCPWC	GPIO2_27	O		3.3	Optional LCD power control
VOU_DEST	GPIO2_3	O		3.3	optional GPIO
SDC1_CMD		I/O		3.3	SDC CMD signal
SDC1_CLK		O		3.3	SDC clock output
SDC1_D[3:0]		I/O		3.3	SDC data
SDC1_CD#	GPIO1_27	I	PU 10K	3.3	SDC card detect input
SDC1_WP	GPIO1_26	I	PD 10K	3.3	SDC write protect input
SPI_SS#		I/O		3.3	SPI Slave select
SPI_SCK		I/O		3.3	SPI Clock
SPI_MISO		I		3.3	Input data from slave
SPI_MOSI		O		3.3	Output data to slave
SCL		O	PU 2K2	3.3	I^2C clock output
SDA		I/O	PU 2K2	3.3	I^2C data signal
AUDIO_BCK		I/O		3.3	PCM bit clock
AUDIO_LRC		I		3.3	PCM L/R signal
AUDIO_DATI		I		3.3	PCM input data
AUDIO_DATO		O		3.3	PCM output data
POWER_ON_BASE		O		3.3	Digital output
GPIO_0	GPIO0_7	I		3.3	Digital I/O
GPIO_1		I	10K PU	3.3	USB1_ID
GPIO_2	GPIO1_21	I/O	10K PU	3.3	Digital I/O, USB1_OC#
GPIO_3		I/O		3.3	USB1_DRVVBUS
GPIO_4	GPIO2_19	I/O		3.3	Digital I/O, UART1_RI
GPIO_5	GPIO3_9	I/O		3.3	Digital I/O, UART1_DCD
GPIO_6	GPIO2_18	I/O		3.3	Digital I/O, UART1_DTR
GPIO_7	GPIO3_10	I/O		3.3	Digital I/O, UART1_DSR
GPIO_8	GPIO0_13	I/O	PU 10K	3.3	Digital I/O, UART1_RTS
GPIO_9	GPIO0_12	I/O		3.3	Digital I/O, UART1_CTS
NMI	GPIO0_6	I	PU 10K	3.3	Interrupt input
IRQ-A	GPIO3_0	I	PU 10K	3.3	Interrupt input
IRQ-B	GPIO2_26	I	PU 10K	3.3	Interrupt input
RESI#		I	PU 10K	3.3	Reset input
RESO#		O	-	3.3	Reset output
BAT		-	-	1.9 … 3.3	Backup battery input for RTC
+3V3		-	-	-	+ 3.3V supply
GND		-	-	-	Ground

5.2 J2, Debug Connector

Name	Direction	Termination	Level [V]	Description
JTAG Interface				
TCK	I		3.3	JTAG clock
TMS	I		3.3	JTAG mode select
TRST#	I	PD 4K7	3.3	JTAG test reset
TDI	I		3.3	JTAG data in
TDO	O		3.3	JTAG data out
SYS_RESIO#	I	PU 4K7	3.3	JTAG reset in/out
Others				
+3V3	-	-	-	+ 3.3V supply
GND	-	-	-	Ground

6 Technical Characteristics

6.1 Electrical Specifications

Supply voltage	3.3 V, +/-5%
Current consumption	0.6 A max.

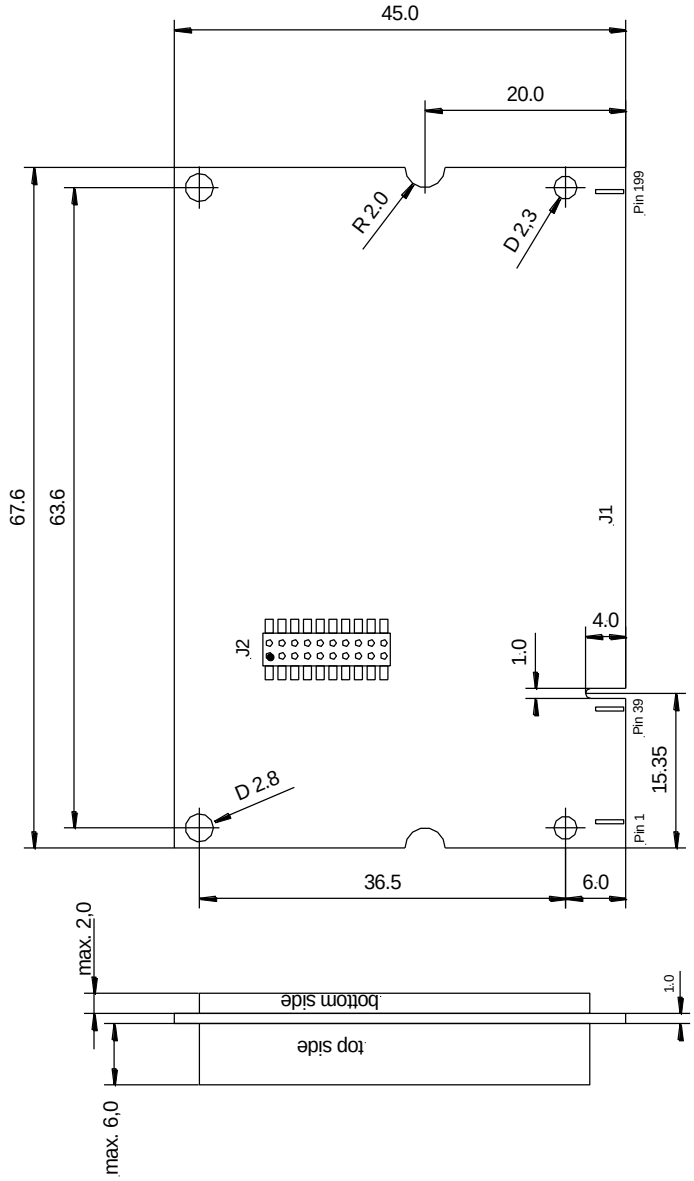
6.2 Environmental Specifications

Operating temperature **Storage temperature**	Standard: 0°C ... +70°C -ET: -40°C ... +85°C -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

6.3 Mechanical Specifications

Weight	approx. 15 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 45.0 mm x 10.0 mm

6.4 Dimensional Drawing



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