DIMM-MX53x

Hardware Manual

Rev6 / 26.09.2018

emtrion GmbH

Revision: **6 / 26.09.2018**

Rev	Date/Signature	Changes
1	02.05.2011	First revision
2	31.05.2011	Added RGB table Added LVDS mapping tables Updated block diagram Changed processor clocks chapter
3	23.09.2011	Address bus extension possibility added Changed RAM memory sizes
4	31.10.2011	Changed Serial Boot Mode interface from UART1 to UART2 Add a description how the DIMM-MX53x module supports DMA accesses. Changed GPIO Port of IRQ1 Changed orientation of J4 in the mechanical drawing. Changed n/c pins of J4 to reserved pins. Changed the signal characteristics tables
5	16.04.2012	Added the 1GB DDR3 support Added the 1GB NAND Flash support Updated the block diagram Added that the processor bus address signals A[10:0] are used for boot configuration. Added the POWER_ON_BASE signal. Added the BAT pin description, updated the BAT pin power supply Updated the mechanical drawings. Updated the Freescale References
6	26.09.2018/We	Added Diameter of mounting holes in mechanical drawings

Contents

1 Introduction

The DIMM-MX53x processor module is a SODIMM sized CPU board based on the i.MX processor i.MX53x from Freescale.

The processor core runs at 800/1000 MHz and it includes a variety of functions required for multimedia or industrial applications. These include a MPEG4 and H.264 encoder, a 3D graphics accelerator, LCD controller, LVDS interface, two camera interfaces, and sound input/output module.

The module can be ordered with different sizes of NAND-Flash and SDRAM. The CPU has an internal Ethernet MAC, two CAN controllers and two USB Controllers, which are used as USB Host and USB Device. Additionally a touch controller is available.

All interfaces are accessible through the 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2,5V keying and two additional extension connectors.

The typical power consumption of the whole board is less than 3W.

In the following table the features and interfaces of the DIMM-MX53x processor module are described.

DIMM-MX53x
256/512MB/1GB SDRAM
256MB to 1GB NAND Flash
Processor Bus (16bit data, 11bit addresses, 1CS)
1x 10/100Mbit Ethernet
1x USB Host
1x USB Device
1x LCD Interface 16/18/24bit max. 1080p (1920x1080)
1x 4 wire Touch
2x Video IN 8bit
1x SSI Audio
1x UART RS232
4x UART LVTTL
IrDA
1x SPI
1x I2C
2x CAN
1x SPDIF in/out
3x IRQ
2x SD Card
4x4 Keypad
1x SATA
1x LVDS 24bit max. WXGA (1366x768)
min. 8 GPIO

Please contact emtrion GmbH for the available NAND Flash and SDRAM Configurations.

UART4 and UART5 can only be used if the Keypad function is not used.

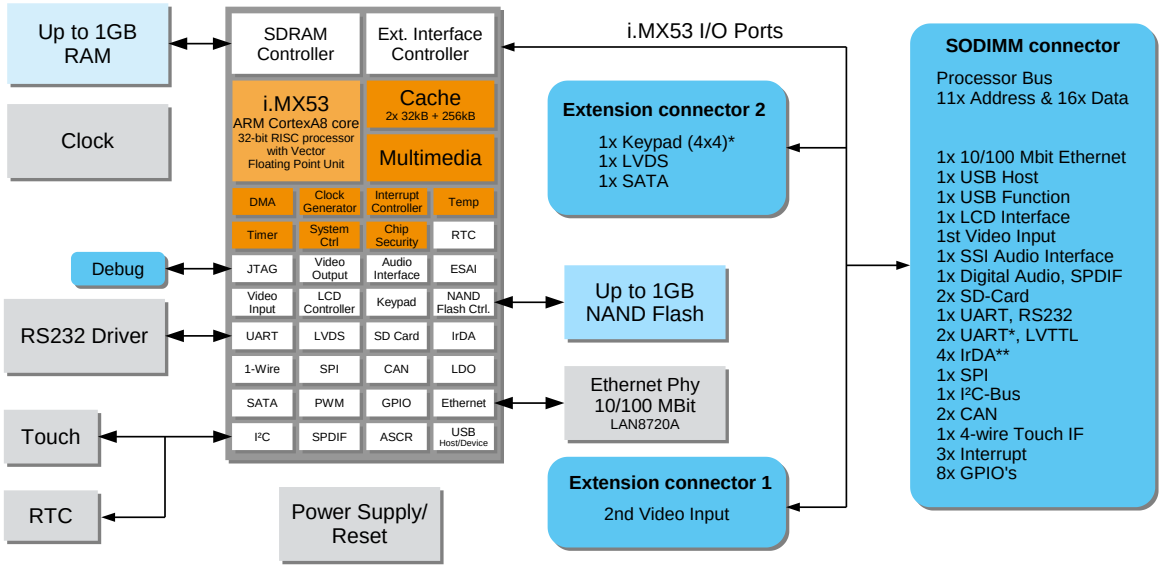
The module is available in standard temperature range 0°C to 70°C and in the extended temperature range -40°C to 85°C.

There are two DIMM-MX53 modules at emtrion GmbH. One is the DIMM-MX537 with the i.MX537 included and the other is the DIMM-MX535 with the i.MX535 included. The most features are similar, but the following table shows the differences between these modules.

feature	DIMM-MX535	DIMM-MX537
Max. Core frequency	1000MHz	800MHz
CAN	n/a	2 ports
Temperature range	0°C to 70°C	0°C to 70°C and -40°C to 85°C
Ethernet	10/100Mbit	10/100Mbit; IEEE1588

2 Block Diagram

The following figure shows the block diagram of the DIMM-MX53x.



* If Keypad not used 2 additional UART's and an additional I2C can be used
** An IrDA port can only be used, if a UART port is not used

3 Handling Precautions

Please read the following notes prior to installing the DIMM-MX53x processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The DIMM-MX53x does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The DIMM-MX53x processor board uses the i.MX processor i.MX53x from Freescale [1], a 32-bit RISC processor which runs at 800/1000MHz.

In addition to the CPU core with MMU, FPU and Caches, this processor provides a lot of features such as:

- Interrupt controller
- Processor Bus Controller with SRAM, PSRAM and NOR Flash interface
- NAND Flash controller
- DDR2 /DDR3SDRAM controller
- 32-bit timer
- 5 UARTs with 2x 32 byte FIFO
- I2C bus interface
- SPI interface
- IrDA interfaces
- Watchdog timer
- Real time clock
- Two Video input modules with camera capturing module and image processing unit
- LCD Controller for TFT displays up to 1080p (1920x1080) @60Hz and 16/18/24 bpp
- 24bit LVDS display port up to WXGA (1366x768) @60Hz and 16/18/24 bpp
- 3D graphic accelerator
- NEON SIMD media accelerator
- 4 wire Touch controller
- Two CAN controllers
- Ethernet MAC 10/100Mbit with IEEE1588 support
- Sound interface with I2S format
- Sound interface SPDIF in and out
- USB 2.0 Host with high-speed mode
- 2 SD Card host controllers
- JTAG debug interface

Further details of the processor can be found in the i.MX53x hardware manual [1].

4.1.1 Processor Clocks

The 24MHz main clock is generated by a quartz crystal. Four internal PLL multiply the 24MHz main clock to the internal clocks. All clocks in processor are derived from theses frequencies, via various software configurable dividers.

The RCLK clock input of the CPU is supplied by a 32,768 kHz clock from the RTC chip and it is used for date and time applications.

4.1.2 Boot Mode

The DIMM-MX53x can boot from the NAND-Flash or serial via USB or UART2. The boot mode is configured via the DIP Switch SW1.

SW1-1	SW1-2	Boot source
0	**0**	NAND-Flash
1	**1**	Serial

Booting from other devices is possible. (Please contact emtrion GmbH)

4.2 NAND-Flash

To store the operating system and application data, a MB NAND Flash is provided. A flash memory MT29FxG from Micron is used and connected to the eight bit NAND Flash controller of the processor.

The NAND Flash size can be 256MB, 512MB and 1GB.

To use the write protect function the WP# Pin of the Flash device is connected to the dedicated WP# pin of the NAND Flash controller of the processor. As default the signal is pulled down and the NAND Flash is protected.

For special applications, the NAND Flash size can be adapted. (Please contact emtrion GmbH)

4.3 DDR2/DDR3 SDRAM

DDR2/DDR3 SDRAM is available as main memory.

The SDRAM size can be 256MB, 512MB and 1GB.

The 256MB RAM is located in the address range 0x70000000 … 0x7FFFFFFF.

The 512MB RAM is located in the address range 0x70000000 … 0x8FFFFFFF.

The 1GB RAM is located in the address range 0x70000000 … 0xAFFFFFFF.

4.4 Processor Bus

The processor bus of the DIMM-MX53x with 16bit data and 11bit addresses is routed to the SODIMM connector. The bus clock, the control signals and one chip select signal is also routed to the SODIMM connector. At this processor bus external devices can be connected.

The processor bus signal level is 3,3V.

The address space is in the range 0xF0000000 … 0xF00007FF.

The following table describes the processor bus interface signals.

signals	description
A[10:0]*	Address bus
D[15:0]	Data bus
CKIO	66 MHz bus clock
WAIT#	Low active wait input signal (must not be used)
CS#	Low active chip select
RD#	Low active read signal
WE0#	Low active low byte D[7:0] selection signal
WE1#	Low active high byte D[15:8] selection signal
RD/WR#	Low active write enable signal

* These signals are used as boot configuration pins during reset. During reset these signals shall not be influenced (e.g. by PU/PD or I/O driver) Please ask emtrion for further information.

The address space of the processor bus can be extended, if the camera interface CSI1 is not needed. The address bus signals are then available on the extension connector 1.

The following table shows the address bus extension and which signals of the CSI1 interface are not available.

address	CSI1 signal	Connector pin
A[11]	CSI1_HSYNC	J3-28
A[12]	CSI1_VSYNC	J3-26
A[13]	DI1_EXT_CLK	J3-21
A[14]	DI0_EXT_CLK	J1-68
A[15]	IRQ2#	J1-186

For that address space growth, the SW must be adapted. Please contact emtrion GmbH, if that feature is useful for you.

If more address space is needed the assembly must be changed. Then the address space can be extended to A[24:0]. Please contact emtrion GmbH for that option

The DIMM-MX53x boards can support DMA accesses. The DMA_REQ signal of the i.MX53x processor is routed to the SODIMM connector, but not to the SODIMM interface pin DREQ (pin 180). The i.MX53x function DMA_REQ shares the SODIMM connector pin 121 with the i.MX53x function SPDIF_OUT. On special or customer baseboards the DMA_REQ can be used at pin 121 of the SODIMM connector.

Contact emtrion GmbH if such a feature is needed.

4.5 Ethernet

The Ethernet interface is realized with the processor internal Media Access Controller (MAC) and an external Physical Layer Interface (PHY) LAN8720A from SMSC. The RMII interface is used for communication between the MAC and the PHY.

The Ethernet interface supports the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. Also HP Auto-MDIX is supported.

The registers of the Ethernet PHY can be configured via the Media Independent Interface (MII).

The Ethernet signal lines (ETH_TDP, ETH_TDM, ETH_RDP, ETH_RDM) as well as two status signals (SPEED_LED#, LINK_LED#) that serve to indicate the link status and the transfer speed are connected to the SODIMM connector. An appropriate 1:1 transformer, which center tap is sourced by 3.3V, must be added externally.

The signal LINK_LED# indicates if data packages are transferred. (“0” = traffic)

The signal SPEED_LED# indicates if the data is transferred with 100Mbit/s. (“0” = 100Mbit/s)

4.6 USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the internal host controller of the i.MX53x. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed, full-speed (12MHz) and high-speed (480Mbps).

To switch the bus power the control line USBH_PEN# is connected to the SODIMM connector. A logical “0” at the processor GPIO1-0 switches the power on; a logical “1” turns the power off. The signal USBH_OC# reports an overcurrent at the GPIO1-3 (“0” = overcurrent).

The data lines and the two control lines are available at the SODIMM connector. A USB power switch must be added externally. The data lines are internally terminated with 15-KΩ pulldown resistors.

The USBH_VBUS signal on the SODIMM connector is only an input, to detect the VBUS voltage on the baseboard.

4.7 USB Device

The USB device port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The interface is realized by the internal device controller of the i.MX53x. The interface is USB 2.0 compliant, supporting data transfers at low-speed, full-speed (12MHz) and high-speed (480Mbps).

The data lines and the control line USBF_VBUS are available at the SODIMM connector.

4.8 Graphic Displays

The DIMM-MX53x has two display ports. One is a 24bit TFT display port and the other is a 24bit LVDS display port. The two ports can display the image or they can display two different images. That can be configured via software.

4.8.1 TFT

The LCD controller of the i.MX53x can drive TFT displays with resolutions up to 1080p (1920x1080) at 16/18/24bpp. The pixel clock for the display data can be generated by an internal clock or via the external DI0_EXT_CLK. Thus all timings can individually be adapted by software to the connected display.

All data and control lines are available at the SODIMM connector. The following table describes the function of the data and control lines.

signals	description
LCD_D[23:0]	24 colour data; can also be used in 18 or 16 bit mode
LCD_VSYNC	Vertical synchronization signal
LCD_HSYNC	horizontal synchronization signal
LCD_DISP	Data enable signal, if active colour data are valid
LCD_PIXCLK	Display clock
DI0_EXT_CLK	External input clock (e.g. spread spectrum oscillator); can be used by the IPU for the display clock;
LCD_DON	Display power enable signal; the display backlight power can be switched (“0” backlight off (default); “1” backlight on)

The following table shows the RGB colour mapping on the LCD_D[23:0] pins of the SODIMM connector.

SODIMM LCD_D[17:0]	RGB565 (16bit)	RGB666 (18bit)	RGB888 (24bit)
LCD_D0	B0	B0	B0
LCD_D1	B1	B1	B1
LCD_D2	B2	B2	B2
LCD_D3	B3	B3	B3
LCD_D4	B4	B4	B4
LCD_D5	G0	B5	B5
LCD_D6	G1	G0	B6
LCD_D7	G2	G1	B7
LCD_D8	G3	G2	G0
LCD_D9	G4	G3	G1
LCD_D10	G5	G4	G2
LCD_D11	R0	G5	G3
LCD_D12	R1	R0	G4
LCD_D13	R2	R1	G5
LCD_D14	R3	R2	G6
LCD_D15	R4	R3	G7
LCD_D16	-	R4	R0

LCD_D17	-	R5	R1
LCD_D18	-	-	R2
LCD_D19	-	-	R3
LCD_D20	-	-	R4
LCD_D21	-	-	R5
LCD_D22	-	-	R6
LCD_D23	-	-	R7

4.8.2 LVDS

The LCD controller of the i.MX53x can drive LVDS with resolutions up to WXGA at 16/18/24bpp. The pixel clock for the display data can be generated by an internal clock or via the external DI0_EXT_CLK. Thus all timings can individually be adapted by software to the connected display.

The LVDS lines are available at the extension connector 2. The following table describes the LVDS signals.

signals	description
LVDS_CLK_P/N	Differential LVDS clock
LVDS_TX0_P/N	First differential LVDS data signal pair
LVDS_TX1_P/N	Second differential LVDS data signal pair
LVDS_TX2_P/N	Third differential LVDS data signal pair
LVDS_TX3_P/N	Fourth differential LVDS data signal pair; only be used in 24bit mode

In the 24 bit mode the colour mapping can be different dependent of the used display. The following table shows the 18/24bit colour mapping in the SPWG/PSWG/VESA mode.

signals	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_TX0	G0	R5	R4	R3	R2	R1	R0
LVDS_TX1	B1	B0	G5	G4	G3	G2	G1
LVDS_TX2	DE	VS	HS	B5	B4	B3	B2
LVDS_TX3 (only for 24bit)	CTL	B7	B6	G7	G6	R7	R6

The following table shows the 24bit colour mapping in the JEIDA mode.

signals	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
LVDS_TX0	G2	R7	R6	R5	R4	R3	R2
LVDS_TX1	B3	B2	G7	G6	G5	G4	G3
LVDS_TX2	DE	VS	HS	B7	B6	B5	B4
LVDS_TX3	CTL	B1	B0	G1	G0	R1	R0

4.9 Touch Interface

A 4-wire touch interface is implemented by using the AR1020 touch interface controller from Microchip [3].

The controller is connected to the I^2C bus interface of the i.MX53x. The IRQ output of the controller is connected to GPIO4-20 of the i.MX53x. The 7-bit I^2C-Address is 0x4D.

The touch interface signals (TOUCH_XP, TOUCH_XM, TOUCH_YP, TOUCH_YM) are available at the SODIMM connector.

4.10 Video Input

The DIMM-MX53x has two video input units (CSIx) which can be used with different video sources, such as video codec or CMOS camera modules.

The CSI0 interface at the DIMM-MX53x is realised with an 8-bit data-bus available at the SODIMM connector and supports various input formats. On some emtrion baseboards the video source can be video codec or a CMOS camera. To switch between the two video sources the signal VIO_SRC (GPIO7-7) is available. To reset the video codec on the base board the signal VIO_RST (GPIO7-6) can be used. Both signals are connected to the SODIMM connector.

The following table describes the CSI0 signals.

signals	description
CSI0_D[7:0]	Video input data
CSI0_CLK	Video input clock
CSI0_HSYNC	Video input horizontal synchronization
CSI0_VSYNC	Video input vertical synchronization
VIO_SRC	Video input source selection; “0” = CMOS camera (default); “1” = video codec
VIO_RST#	Video input source reset; “0” = reset; “1” = no reset (default)

The CSI1 interface at the DIMM-MX53x is realised with an 8-bit data-bus available at the extension connector 1 and it supports various input formats.

The following table describes the CSI1 signals.

signals	description
CSI1_D[7:0]	Video input data
CSI1_CLK	Video input clock
CSI1_HSYNC	Video input horizontal synchronization
CSI1_VSYNC	Video input vertical synchronization

4.11 Audio Interfaces

4.11.1 Audio SSI

The i.MX53x processor has an integrated Audio module that can be used to send and receive audio data from external audio codecs.

The interface is connected to SODIMM connector, which allows the selection of an external audio codec.

4.11.2 Audio SPDIF

The DIMM-MX53x also supports the SPDIF format. The input and output pins at the SODIMM connector have LVTTL level and will need to be configured external according to the SPDIF specifications.

4.12 SD-Card Interface

The i.MX53x includes two SD Card interfaces to drive memory- or I/O cards. The signals, including card detect and write protect lines, are routed with all necessary pull up resistors to the SODIMM connector.

The card detect and write protect signals are handled by GPIO pins of the i.MX53x:

Signal	Function	GPIO	Remarks
SDC1_CD#	Low-active card detection signal	GPIO1-1	Pullup resistor added
SDC1_WP	high-active write protection signal	GPIO1-9	Pullup resistor added
SDC2_CD#	Low-active card detection signal	GPIO1-4	Pullup resistor added
SDC2_WP	high-active write protection signal	GPIO1-2	Pullup resistor added

4.13 Serial Ports

The DIMM-MX53x has five serial ports. All serial ports are integrated in the processor i.MX53x.

An overview of the UART interfaces is shown as follows:

i.MX53x interface	SODIMM name	handshake signals	Signal level
UART1	UART_A	RTS, CTS	RS232
UART2	UART_B	-	LVTTL
UART3	UART_C	-	LVTTL
UART4	UART_D	-	LVTTL
UART5	UART_E	-	LVTTL

On DIMM-MX53x-2 and DIMM-MX53x-1 boards RTS and CTS of UART1 are not supported.

RS232 adaptors that can be plugged to a pin header are available from emtrion GmbH.

UART4 and UART5 can only be used if the Keypad function is not used.

4.14 IrDA

Each UART port can also be used as low speed (115200bps) Infrared port (IrDA). So on the DIMM-MX53x there is the possibility of 4 IrDA ports. UART1 can't be used as IrDA port, because of the RS232 driver onboard. The UART RXD input signal is also the IrDA RXD input signal. The UART TXD output signal is also the IrDA TXD output signal.

4.15 I^2C- Bus

The i.MX53x provides an I^2C bus interface with transmission speeds up to 100 kb/s. The interface operates as a master.

Two devices are connected to the bus on DIMM-MX53x:

Slave	Device	Chip Address
Real Time Clock	DS1337U+	0x68
Touch controller	AR1020	0x4D

The bus connects to the SODIMM connector. The SCL and SDA lines are pulled up with 2,2kΩ resistors to 3,3V.

4.16 SPI Interface

The SPI interface of the i.MX53x processor is connected to the SODIMM connector. The four signals SPI_SCK, SPI_CS#, SPI_MOSI and SPI_MISO are routed to the SODIMM connector.

4.17 CAN

The i.MX537 includes two CAN controllers. The TX and RX signals are routed with all necessary pull up resistors to the SODIMM connector. For each CAN interface a CAN transceiver must be realized on the base board.

The signal level is 3,3V.

The i.MX535 doesn't support CAN.

4.18 SATA

The i.MX53x includes a SATA controller and a SATA phy. The SATA controller is compliant with the SATA specification 2.6 at 1,5Gb/s.

The SATA signals are routed to the extension connector 2.

Further details of the SATA controller can be found in the i.MX53x hardware manual [1].

4.19 Keypad

The i.MX53x includes a Keypad port. A 4x4 Keypad matrix can be realized.

The SATA signals are routed to the extension connector 2.

Keypad function can only be used if UART4 and UART5 are not used.

4.20 General Purpose I/Os

Eight port pins of the processor which can be used as GPIOs are routed to the SODIMM connector.

SIGNAL	i.MX53x Port	Direction
GPIO_A	GPIO2-8	In/Out
GPIO_B	GPIO2-9	In/Out
GPIO_C	GPIO2-10	In/Out
GPIO_D	GPIO2-11	In/Out
GPIO_E	GPIO2-12	In/Out
GPIO_F	GPIO2-13	In/Out
GPIO_G	GPIO2-14	In/Out
GPIO_H	GPIO2-15	In/Out

The signal level of each GPIO pin is 3,3V.

4.21 DIP Switches, Status LED

Two DIP switches are on the DIMM-MX53x. Via that DIP switches the boot mode of the DIMM-MX53x module can be configured. If a switch is ON the corresponding bit is read as 1. If it is OFF the bit is read as 0. The following table describes the boot mode options.

SW1	SW2	Boot Mode
OFF	OFF	NAND Flash Boot
ON	ON	USB/UART Serial Boot

Further details of the boot mode options can be found in the i.MX53x hardware manual [1].

A bicolour LED is connected to the port pins GPIO4-3 and GPIO4-4 of the i.MX53x. If GPIO4-3 is high a green LED is lighting, if GPIO4-4 is high a red LED is lighting. If both ports are high both LEDs are on, which results in a yellow light.

4.22 Memory Map

In the following table the memory spaces of the external memory or devices is shown.

Function	Bus Width	Address Region
256 MB SDRAM	32-bit	0x70000000 – 0x7FFFFFFF
512 MB SDRAM	32-bit	0x70000000 – 0x8FFFFFFF
1 GB SDRAM*	32-bit	0x70000000 – 0xAFFFFFFF
SODIMM	8/16-bit	0xF0000000 – 0xF00007FF

* The 1GB SDRAM is only available on DIMM-MX53x-3 boards.

The timing characteristics of DDR SDRAM area is programmed according to the requirements of the DIMM-MX53x processor board.

The SODIMM area is reserved for external extensions and therefore configured with the slowest timing.

4.23 Interrupts

The processor i.MX53x has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor.

Each GPIO Input can be configured as an interrupt input.

The use of the interrupt inputs is shown in the following table:

GPIO Port	Source
GPIO5-2*	SODIMM (IRQ1)
GPIO3-15	SODIMM (IRQ2)
GPIO2-24	SODIMM (IRQ3)
GPIO4-2	DS1337

GPIO4-20	AR1020

*The i.MX53 GPIO Port of the signal IRQ1 has changed between board revision R1 and R2. On R1 boards (DIMM-MX53x-1) the GPIO Port of IRQ1 is GPIO2-30.

The signal level of each interrupt is 3,3V.

4.24 Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the board voltages. (POR#)
- Via the active low signal RESI# at the SODIMM connector. (RESET_IN#)
- Via the active low signal JTAG_RESI# at the Debug connector. (RESET_IN#)
- Via the board signal HRESET_B and the processor function SYSTEM_RST. (RESET_IN#)

All resets are hardware resets of the whole board. The POR# reset issue a processor cold reset. The RESET_IN# reset issue a processor warm reset.

The duration of the reset signal is min. 140ms. For resetting external devices the reset signal is available as an output (RESO#) at the SODIMM connector.

4.25 Power Supply

The max power consumption is 1A at +3,3V, +/- 5%, which must be supplied via the SODIMM connector. Further voltages for the processor and the other parts are generated on board.

On DIMM-MX53x-3 boards the output signal POWER_ON_BASE is available on the SODIMM pin 135. This signal is an output signal of the DIMM-MX53x-3 board. The POWER_ON_BASE signal can be used on the baseboard to switch on the power supply of the connected periphery components. With that signal the DIMM-MX53x-3 board can control when the power supply of the baseboard periphery components are powered on. POWER_ON_BASE is a HW controlled signal and can't be configured by SW. The following table describes the logic of the POWER_ON_BASE signal.

POWER_ON_BASE	Baseboard Periphery power supply
0	off
1	on

If the baseboard doesn't support that feature a protection circuit on the DIMM module avoids a shortcut if on the baseboard +3V3 is supply on the SODIMM pin 135.

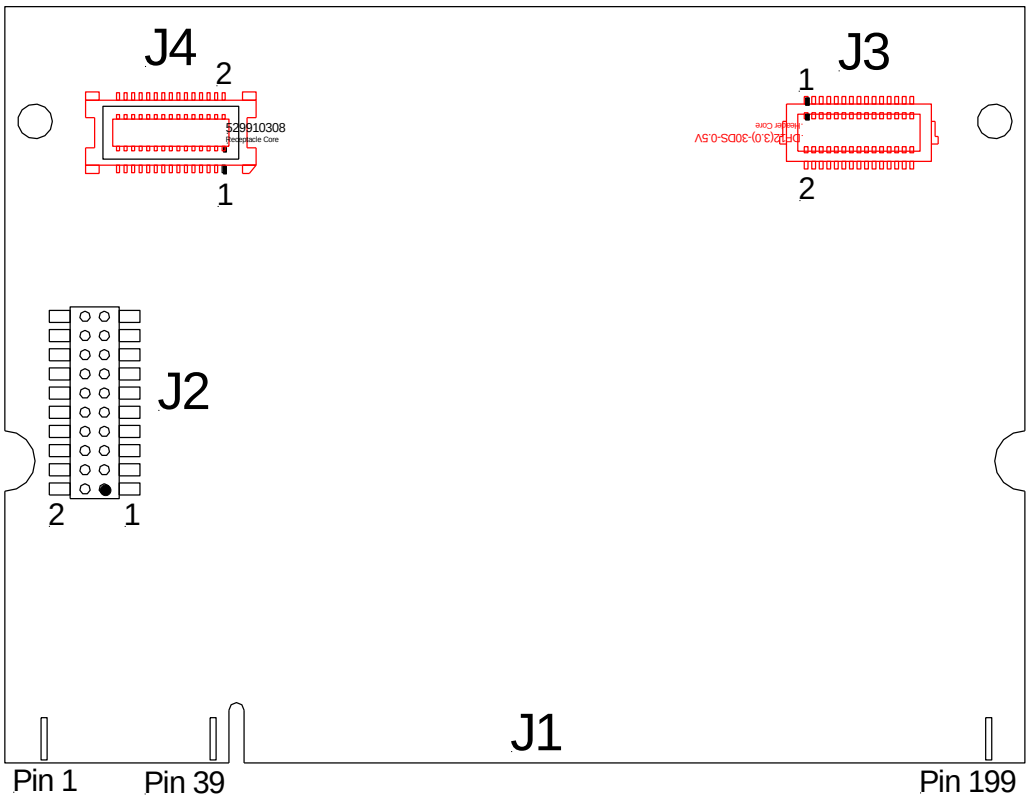
For more information about that feature see the Application Note Baseboard-Design on the emtrion support Homepage http://www.support.emtrion.de/doku.php?id=hw:dimmconcept or contact emtrion GmbH.

On DIMM-MX53x-2 boards the SODIMM pin 135 is used as +3V3 power supply input pin.

The SODIMM BAT pin is the battery input pin for the RTC power supply. The typical power consumption of the RTC via the BAT pin is < 1µA.

4.26 Connectors

On the DIMM-MX53x there are 4 connectors. J1 is the main SODIMM connector. J2 is the JTAG debug connector. J3 and J4 are extension connectors.



Red colored parts are located on the bottom side of the CPU module.

4.26.1 DIMM Interface

The most interface signals of the board are available at the SODIMM connector.

The DIMM interface is a 200 pos SODIMM connector that fits mechanically into a regular DDR1 SODIMM memory socket with 2,5V keying. These sockets are available from various manufacturers.

Usage details of the connector and its electrical and mechanical characteristics can be found later in this document.

Notes:

The pin out of the SODIMM connector is NOT compatible with memory sockets. Insertion into a socket with wrong pin out may damage the DIMM-MX53x and the carrier board.

Most of the pins are directly connected with the processor i.MX53x.

4.26.2 Debugging interface

At the 20 pole header J2 all signals of the ARM debug interface and the Boot Mode signals are available.

Please contact emtrion GmbH for further details how to connect an emulator to J2.

4.26.3 Extension Interface

The interfaces CSI1, LVDS, SATA and keypad are routed to the extension connectors. More details about the pin assignment and the connector types are described in chapter 5.2 and 5.3.

5 Pin Assignments

5.1 J1, SODIMM

Type SODIMM, 200 pos, 2,5V keying

Pin	Signal	Interface		Signal	Pin
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2
3	ETH_TDP			USBH_OC#	4
5	ETH_TDM			USBH_DM	6
7	GND			USBH_DP	8
9	ETH_RDP		USB Device	USBF_VBUS	10
11	ETH_RDM			USBF_DM	12
13	LINK_LED#			USBF_DP	14
15	USBH_VBUS	USB Host	Power	GND	16
17	CAN1_TX	CAN	UART-A	UART1_TXD#	18
19	CAN1_RX			UART1_RXD#	20
21	UART5_TXD	UART-E		UART1_RTS#	22
23	UART5_RXD			UART1_CTS#	24
25	UART4_TXD	UART-D	Touch	Touch_XP	26
27	UART4_RXD			Touch_XM	28
29	UART3_TXD	UART-C		Touch_YP	30
31	UART3_RXD			Touch_YM	32
33	UART2_TXD	UART-B	A/D	n/c	34
35	UART2_RXD			n/c	36
37	n/c	A/D		n/c	38
39	+3V3	Power		GND	40
41	LCD_D22*	LCD		LCD_D23*	42
43	LCD_D20*			LCD_D21*	44
45	LCD_D18 *			LCD_D19*	46
47	LCD_D16			LCD_D17	48
49	LCD_D14			LCD_D15	50
51	LCD_D12			LCD_D13	52

53	LCD_D10			LCD_D11	**54**
55	LCD_D8			LCD_D9	**56**
57	LCD_D6			LCD_D7	**58**
59	LCD_D4			LCD_D5	**60**
61	LCD_D2			LCD_D3	**62**
63	LCD_D0			LCD_D1	**64**
65	+3V3	**Power**		GND	**66**
67	n/c	**LCD**		DI0_EXT_CLK	**68**
69	LCD_DISP			LCD_DCK	**70**
71	LCD_HSYN			LCD_DON	**72**
73	LCD_VSYN			LCD_VCPWC*	**74**
75	VOU_DEST**			LCD_VEPWC*	**76**
77	VOU_RST#	**VIO0, VOU**		CSI0_D7	**78**
79	n/c			CSI0_D6	**80**
81	n/c			CSI0_D5	**82**
83	CSI0_PIXCLK			CSI0_D4	**84**
85	CSI0_HSYNC			CSI0_D3	**86**
87	CSI0_VSYNC			CSI0_D2	**88**
89	VIO_SRC			CSI0_D1	**90**
91	VIO_RST#			CSI0_D0	**92**
93	+3V3	**Power**		GND	**94**
95	SDC2_D0	**SDC2**	**SDC1**	SDC1_D0	**96**
97	SDC2_D1			SDC1_D1	**98**
99	SDC2_D2			SDC1_D2	**100**
101	SDC2_D3			SDC1_D3	**102**
103	SDC2_CMD			SDC1_CMD	**104**
105	SDC2_CLK			SDC1_CLK	**106**
107	SDC2_CD#			SDC1_CD#	**108**
109	SDC2_WP			SDC1_WP	**110**
111	SPI_SS#	**SPI**		SPI_MISO	**112**
113	SPI_SCK			SPI_MOSI	**114**

115	SCL	**I2C**	**Audio**	AUDIO_BCK	**116**
117	SDA			AUDIO_LRC	**118**
119	SPDIF_IN	**SPDIF**		AUDIO_DATI	**120**
121	SPDIF_OUT			AUDIO_DATO	**122**
123	GND	**Power**		n/c	**124**
125	CAN2_RX	**GPIO,TPU**		CAN2_TX	**126**
127	GPIO_G			GPIO_H/	**128**
129	GPIO_E			GPIO_F	**130**
131	GPIO_C			GPIO_D	**132**
133	GPIO_A			GPIO_B	**134**
135	POWER_ON_BASE***	**Power**		GND	**136**
137	n/c	**Address A[23:0]**		n/c	**138**
139	n/c			n/c	**140**
141	n/c			n/c	**142**
143	n/c			n/c	**144**
145	n/c			n/c	**146**
147	n/c			n/c	**148**
149	A10****			n/c	**150**
151	A8****			A9****	**152**
153	A6****			A7****	**154**
155	A4****			A5****	**156**
157	A2****			A3****	**158**
159	A0****			A1****	**160**
161	+3V3	**Power**		GND	**162**
163	D14	**Data D[15:0]**		D15	**164**
165	D12			D13	**166**
167	D10			D11	**168**
169	D8			D9	**170**
171	D6			D7	**172**
173	D4			D5	**174**
175	D2			D3	**176**

177	D0			D1	**178**
179	PB_CLK			n/c	**180**
181	n/c			DACK**	**182**
183	RD#			IRQ1#	**184**
185	RD/WR#			IRQ2#	**186**
187	WE0#			IRQ3#	**188**
189	WE1#			RESO#	**190**
191	n/c			RESI#	**192**
193	n/c			n/c	**194**
195	WAIT#			n/c	**196**
197	PB_CS#			n/c	**198**
199	BAT	**Power**		GND	**200**

Bus Control

* These signals are not available by default. Please ask emtrion for further information.

** These have no function with DIMM-MX53x. They are pulled-down or pulled up.

*** This signal is only available on DIMM-MX53x-3 boards. On DIMM-MX53x-2 boards this pin is used +3V3 power supply input.

**** These signals are used as boot configuration pins during reset. During reset these signals shall not be influenced (e.g. by PU/PD or I/O driver) Please ask emtrion for further information.

5.2 J3, Extension Connector 1

Type 30-pin connector, Hirose DF12(3.0)-30DS-0.5V (Receptacle)
Corresponding header for base boards: Hirose DF12(3.0)-30DP-0.5V

Pin	Signal	Pin	Signal
1	GND	**2**	n/c
3	n/c	**4**	CSI1_D7
5	n/c	**6**	CSI1_D6
7	n/c	**8**	CSI1_D5
9	n/c	**10**	CSI1_D4
11	n/c	**12**	CSI1_D3
13	n/c	**14**	CSI1_D2
15	n/c	**16**	CSI1_D1

17	n/c	**18**	CSI1_D0
19	GND	**20**	GND
21	DI1_EXT_CLK	**22**	CSI1_PIXCLK
23	n/c	**24**	n/c
25	n/c	**26**	CSI1_VSYNC
27	n/c	**28**	CSI1_HSYNC
29	GND	**30**	n/c

5.3 J4, Extension Connector 2

Type 30-pin connector, Molex 529910308 (Receptacle)
Corresponding header for base boards: Molex 537480308

Pin	Signal	Pin	Signal
1	SATA_RXN	**2**	LVDS_TX2_N
3	SATA_RXP	**4**	LVDS_TX2_P
5	SATA_TXP	**6**	LVDS_TX0_N
7	SATA_TXN	**8**	LVDS_TX0_P
9	GND	**10**	GND
11	KPP_ROW1	**12**	LVDS_TX1_N
13	KPP_COL1	**14**	LVDS_TX1_P
15	KPP_ROW0	**16**	GND
17	KPP_COL0	**18**	LVDS_CLK_N
19	KPP_ROW2	**20**	LVDS_CLK_P
21	KPP_ROW3	**22**	GND
23	KPP_COL3	**24**	LVDS_TX3_N
25	KPP_COL2	**26**	LVDS_TX3_P
27	reserved	**28**	GND
29	reserved	**30**	reserved

5.4 J2, Debugging Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	RTCK	2	TCK
3	GND	4	GND
5	+2V8	6	TRST#
7	+3V3	8	+3V3
9	n/c	10	TDO
11	BOOT_MODE1	12	JTAG_DE#
13	BOOT_MODE0	14	TMS
15	JTAG_MODE	16	TDI
17	GND	18	DBG_ACK
19	JTAG_RESI#	20	JTAG_RESET#

6 Signal Characteristics

Abbreviations:

AI	analogue input
AO	analogue output
A I/O	analogue bidirectional
I	digital input
O	digital output
I/O	digital bidirectional
O(OD)	digital open drain output

PU xK	x KΩ pullup resistor
PD xK	x KΩ pulldown resistor
SR xR	x Ω series resistor
IPU xK	processor internal x KΩ pullup resistor
IPD xK	transistor internal x KΩ pulldown resistor

6.1 J1, SODIMM Connector

Name	i.MX53 Pad Name	GPIO	Direction	Add. Wiring at Reset	Volt [V]	Description
Ethernet						
SPEED_LED#			O(OD)	-	3,3	100 Mbit indicator
ETH_TDP			AO	-	-	TX diff. output pos.
ETH_TDM			AO	-	-	TX diff. output neg.
ETH_RDP			AI	-	-	RX diff. input pos.
ETH_RDN			AI	-	-	RX diff. input neg.
LINK_LED#			O(OD)	-	3,3	traffic indicator

USB Host						
USBH_PEN#	GPIO_0	GPIO1-0	O	PU 10K	3,3	USB power enable signal for power switch
USBH_OC#	GPIO_3	GPIO1-3	I	IPD 360K	3,3	USB overcurrent signal from power switch
USBH_DP	USB_H1_DP		I/O	IPU 15K	5	Diff. data positive
USBH_DM	USB_H1_DN		I/O	IPU 15K	5	Diff. data negative
USBH_VBUS	USB_H1_VBUS		I	-	5	VBUS detection
USB Device						
USBF_VBUS	USB_OTG_VBUS		I	-	5	VBUS detection
USBF_DP	USB_OTG_DP		I/O	-	5	Diff. data positive
USBF_DM	USB_OTG_DN		I/O	-	5	Diff. data negative
UART						
UART1_TXD#			O	-	RS232	RS232 transmit data
UART1_RXD#			I	-	RS232	RS232 receive data
UART1_RTS#			O	-	RS232	RS232 modem control
UART1_CTS#			I	-	RS232	RS232 modem control
UART2_TXD	PATA_DMARQ	GPIO7-0	O	IPU 100K	3,3	transmit data
UART2_RXD	PATA_BUFFER_EN	GPIO7-2	I	IPU 100K / SR1k	3,3	receive data
UART3_TXD	PATA_CS0	GPIO7-9	O	IPU 100K	3,3	transmit data
UART3_RXD	PATA_CS1	GPIO7-10	I	IPU 100K / SR1k	3,3	receive data
UART4_TXD	KEY_COL0	GPIO4-6	O	IPU 100K	3,3	transmit data
UART4_RXD	KEY_ROW0	GPIO4-7	I	IPD 360K / SR1k	3,3	receive data
UART5_TXD	KEY_COL1	GPIO4-8	O	IPU 100K	3,3	transmit data
UART5_RXD	KEY_ROW1	GPIO4-9	I	IPU 100K / SR1k	3,3	receive data
CAN						
CAN1_TX	PATA_INTRQ	GPIO7-2	O	IPU 100K	3,3	transmit data
CAN1_RX	PATA_DIOR	GPIO7-3	I	IPU 100K / SR1k	3,3	receive data
CAN2_TX	KEY_COL4	GPIO4-14	O	IPU 100K	3,3	transmit data
CAN2_RX	KEY_ROW4	GPIO4-15	I	IPD 360K / SR1k	3,3	receive data

4-Wire Resistive Touch Interface						
TOUCH_XP			A I/O	-	3,3	X plus terminal
TOUCH_XM			A I/O	-	3,3	X minus terminal
TOUCH_YP			A I/O	-	3,3	Y plus terminal
TOUCH_YM			A I/O	-	3,3	Y minus terminal
LCD (Graphic Display)						
LCD_DON	GPIO_7	GPIO1-7	O	IPD 360K	2,8	LCD display enable signal
LCD_DISP	DI0_PIN15	GPIO4-17	O	IPU 100K	2,8	LCD data enable signal
LCD_VSYNC	DI0_PIN3	GPIO4-19	O	IPU 100K	2,8	LCD frame sync output
LCD_HSYNC	DI0_PIN2	GPIO4-18	O	IPU 100K	2,8	LCD line sync output
LCD_D0	DISP0_DAT0	GPIO4-21	O	IPD 100K	2,8	LCD colour data
LCD_D1	DISP0_DAT1	GPIO4-22	O	IPD 100K	2,8	LCD colour data
LCD_D2	DISP0_DAT2	GPIO4-23	O	IPD 100K	2,8	LCD colour data
LCD_D3	DISP0_DAT3	GPIO4-24	O	IPD 100K	2,8	LCD colour data
LCD_D4	DISP0_DAT4	GPIO4-25	O	IPD 100K	2,8	LCD colour data
LCD_D5	DISP0_DAT5	GPIO4-26	O	IPD 100K	2,8	LCD colour data
LCD_D6	DISP0_DAT6	GPIO4-27	O	IPD 100K	2,8	LCD colour data
LCD_D7	DISP0_DAT7	GPIO4-28	O	IPD 100K	2,8	LCD colour data
LCD_D8	DISP0_DAT8	GPIO4-29	O	IPU 100K	2,8	LCD colour data
LCD_D9	DISP0_DAT9	GPIO4-30	O	IPU 100K	2,8	LCD colour data
LCD_D10	DISP0_DAT10	GPIO4-31	O	IPU 100K	2,8	LCD colour data
LCD_D11	DISP0_DAT11	GPIO5-5	O	IPD 100K	2,8	LCD colour data
LCD_D12	DISP0_DAT12	GPIO5-6	O	IPU 100K	2,8	LCD colour data
LCD_D13	DISP0_DAT13	GPIO5-7	O	IPU 100K	2,8	LCD colour data
LCD_D14	DISP0_DAT14	GPIO5-8	O	IPU 100K	2,8	LCD colour data
LCD_D15	DISP0_DAT15	GPIO5-9	O	IPU 100K	2,8	LCD colour data
LCD_D16	DISP0_DAT16	GPIO5-10	O	IPU 100K	2,8	LCD colour data
LCD_D17	DISP0_DAT17	GPIO5-11	O	IPU 100K	2,8	LCD colour data
LCD_D18	DISP0_DAT18	GPIO5-12	O	IPU 100K	2,8	LCD colour data
LCD_D19	DISP0_DAT19	GPIO5-13	O	IPU 100K	2,8	LCD colour data
LCD_D20	DISP0_DAT20	GPIO5-14	O	IPU 100K	2,8	LCD colour data

LCD_D21	DISP0_DAT21	GPIO5-15	O	IPU 100K	2,8	LCD colour data
LCD_D22	DISP0_DAT22	GPIO5-16	O	IPU 100K	2,8	LCD colour data
LCD_D23	DISP0_DAT23	GPIO5-17	O	IPU 100K	2,8	LCD colour data
LCD_PIXCLK	DI0_DISP_CLK	GPIO4-16	O	IPU 100K	2,8	LCD data clock
DI0_EXT_CLK	EIM_DA14	GPIO3-14	I	IPU 100K	3,3	External Reference clock for LCD
LCD_VCPWC	GPIO_8	GPIO1-8	O	IPD 360k	3,3	Reserved LCD signal, can be used as GPIO
LCD_VEPWC	CSI0_DATA_EN	GPIO5-20	O	IPU 100K	3,3	Reserved LCD signal, can be used as GPIO
VOU_RST#	PATA_DA2	GPIO7-8	O	PD 1k	3,3	Can be used for SW controllable reset signal or GPIO
CSIO (Video Input Unit 0)						
CSI0_D0	CSI0_DAT12	GPIO5-30	I	PD 100K	3,3	Video input data
CSI0_D1	CSI0_DAT13	GPIO5-31	I	IPD 100K	3,3	Video input data
CSI0_D2	CSI0_DAT14	GPIO6-0	I	IPD 100K	3,3	Video input data
CSI0_D3	CSI0_DAT15	GPIO6-1	I	IPD 100K	3,3	Video input data
CSI0_D4	CSI0_DAT16	GPIO6-2	I	IPD 100K	3,3	Video input data
CSI0_D5	CSI0_DAT17	GPIO6-3	I	IPD 100K	3,3	Video input data
CSI0_D6	CSI0_DAT18	GPIO6-4	I	IPD 100K	3,3	Video input data
CSI0_D7	CSI0_DAT19	GPIO6-5	I	IPD 100K	3,3	Video input data
CSI0_CLK	CSI0_PIXCLK	GPIO5-18	I	IPU 100K	3,3	Video clock input
CSI0_HSYNC	CSI0_MCLK	GPIO5-19	I	IPU 100K	3,3	Video hsync input
CSI0_VSYNC	CSI0_VSYNC	GPIO5-21	I	IPU 100K	3,3	Video vsync input
VIO_SRC	PATA_DA1	GPIO7-7	O	IPU 100K	3,3	Selection of either camera or video codec input
VIO_RST#	PATA_DA0	GPIO7-6	O	PD 1K	3,3	Reset signal for video device
SPI						
SPI_CS#	CSI0_DAT11	GPIO5-29	O	IPU 100K	3,3	Chip select output
SPI_SCK	CSI0_DAT8	GPIO5-26	O	IPU 100K	3,3	Clock output
SPI_MISO	CSI0_DAT10	GPIO5-28	I	IPU 100K / SR1k	3,3	Input data from slave
SPI_MOSI	CSI0_DAT9	GPIO5-27	O	IPD 360K	3,3	Output data to slave
SD Card Interface						
SDC1_D0	SD1_DAT0	GPIO1-16	I/O	IPU 100K	3,3	SDC data

SDC1_D1	SD1_DAT1	GPIO1-17	I/O	IPU 100K	3,3	SDC data
SDC1_D2	SD1_DAT2	GPIO1-19	I/O	IPU 100K	3,3	SDC data
SDC1_D3	SD1_DAT3	GPIO1-21	I/O	IPU 100K	3,3	SDC data
SDC1_CMD	SD1_CMD	GPIO1-18	I/O	IPU 100K	3,3	CMD signal
SDC1_CLK	SD1_CLK	GPIO1-20	O	IPU 100K	3,3	SDC Clock output
SDC1_CD#	GPIO_1	GPIO1-1	I	PU 10K	3,3	Card detect input
SDC1_WP	GPIO_2	GPIO1-9	I	IPU 100K	3,3	Write protect input
SDC2_D0	SD2_D0	GPIO1-15	I/O	IPU 100K	3,3	SDC data
SDC2_D1	SDC_D1	GPIO1-14	I/O	IPU 100K	3,3	SDC data
SDC2_D2	SD2_D2	GPIO1-13	I/O	IPU 100K	3,3	SDC data
SDC2_D3	SD2_D3	GPIO1-12	I/O	IPU 100K	3,3	SDC data
SDC2_CMD	SD2_CMD	GPIO1-11	I/O	IPU 100K	3,3	CMD signal
SDC2_CLK	SD2_CLK	GPIO1-10	O	IPU 100K	3,3	SDC Clock output
SDC2_CD#	GPIO_4	GPIO1-4	I	IPU 100K	3,3	Card detect input
SDC2_WP	GPIO_2	GPIO1-2	I	PU 10K	3,3	Write protect input
I2C						
SCL	GPIO_5	GPIO1-5	I/O	PU 2K2	3,3	I^2C clock signal
SDA	GPIO_6	GPIO1-6	I/O	PU 2K2	3,3	I^2C data signal
Audio SSI						
AUDIO_BCK	CSI0_DAT4	GPIO5-22	I/O	IPU 100K / SR1k	3,3	Sound bit clock
AUDIO_LRC	CSI0_DAT6	GPIO5-24	I	IPU 100K / SR1k	3,3	Sound L/R signal
AUDIO_DATI	CSI0_DAT7	GPIO5-25	I	IPU 100K / SR1k	3,3	Sound serial input data
AUDIO_DATO	CSI0_DAT5	GPIO5-23	O	IPD 360K / SR1k	3,3	Sound serial output data
Audio SPDIF						
SPDIF_IN	GPIO_16	GPIO7-11	I	IPD 360K / SR1k	3,3	SPDIF sound serial input data
SPDIF_OUT	GPIO_17	GPIO7-12	O	IPD 360K	3,3	SPDIF Sound serial output data
General Purpose I/O						
GPIOA	PATA_DATA8	GPIO2-8	I/O	IPU 100K / SR1k	3,3	digital input / output
GPIOB	PATA_DATA9	GPIO2-9	I/O	IPU 100K / SR1k	3,3	digital input / output
GPIOC	PATA_DATA10	GPIO2-10	I/O	IPU 100K / SR1k	3,3	digital input / output
GPIOD	PATA_DATA11	GPIO2-11	I/O	IPU 100K / SR1k	3,3	digital input / output

GPIOE	PATA_DATA12	GPIO2-12	I/O	IPU 100K / SR1k	3,3	digital input / output
GPIOF	PATA_DATA13	GPIO2-13	I/O	IPU 100K / SR1k	3,3	digital input / output
GPIOG	PATA_DATA14	GPIO2-14	I/O	IPU 100K / SR1k	3,3	digital input / output
GPIOH	PATA_DATA15	GPIO2-15	I/O	IPU 100K / SR1k	3,3	digital input / output
Bus Interface						
A0	EIM_DA0	GPIO3-0	O	PD 10K[1]	3,3	Processor address bus
A1	EIM_DA1	GPIO3-1	O	PD 10K[1]	3,3	Processor address bus
A2	EIM_DA2	GPIO3-2	O	PU 10K[1]	3,3	Processor address bus
A3	EIM_DA3	GPIO3-3	O	PD 10K[1]	3,3	Processor address bus
A4	EIM_DA4	GPIO3-4	O	PD 10K[1]	3,3	Processor address bus
A5	EIM_DA5	GPIO3-5	O	PD 10K[1]	3,3	Processor address bus
A6	EIM_DA6	GPIO3-6	O	PU 10K[1]	3,3	Processor address bus
A7	EIM_DA7	GPIO3-7	O	PD 10K[1]	3,3	Processor address bus
A8	EIM_DA8	GPIO3-8	O	PD 10K[1]	3,3	Processor address bus
A9	EIM_DA9	GPIO3-9	O	PD 10K[1]	3,3	Processor address bus
A10	EIM_DA10	GPIO3-10	O	PU 10K[1]	3,3	Processor address bus
D0	EIM_D16	GPIO3-16	I/O	IPU 100K	3,3	Processor data bus
D1	EIM_D17	GPIO3-17	I/O	IPU 100K	3,3	Processor data bus
D2	EIM_D18	GPIO3-18	I/O	IPU 100K	3,3	Processor data bus
D3	EIM_D19	GPIO3-19	I/O	IPU 100K	3,3	Processor data bus
D4	EIM_D20	GPIO3-20	I/O	IPU 100K	3,3	Processor data bus
D5	EIM_D21	GPIO3-21	I/O	IPU 100K	3,3	Processor data bus
D6	EIM_D22	GPIO3-22	I/O	IPD 360K	3,3	Processor data bus
D7	EIM_D23	GPIO3-23	I/O	IPU 100K	3,3	Processor data bus
D8	EIM_D24	GPIO3-24	I/O	IPU 100K	3,3	Processor data bus
D9	EIM_D25	GPIO3-25	I/O	IPU 100K	3,3	Processor data bus
D10	EIM_D26	GPIO3-26	I/O	IPU 100K	3,3	Processor data bus
D11	EIM_D27	GPIO3-27	I/O	IPU 100K	3,3	Processor data bus
D12	EIM_D28	GPIO3-28	I/O	IPU 100K	3,3	Processor data bus
D13	EIM_D29	GPIO3-29	I/O	IPU 100K	3,3	Processor data bus
D14	EIM_D30	GPIO3-30	I/O	IPU 100K	3,3	Processor data bus

D15	EIM_D31	GPIO3-31	I/O	IPD 360K	3,3	Processor data bus
CKIO	EIM_BCLK		O		3,3	66 MHz bus clock
WAIT#	EIM_WAIT	GPIO5-0	I	IPU 100K	3,3	Wait Input
CS#	EIM_CS0	GPIO2-23	O	IPU 100K	3,3	Chip select output
RD#	EIM_OE	GPIO2-25	O	IPU 100K	3,3	Read signal
WE0#	EIM_EB2	GPIO2-30	O	IPU 100K	3,3	Write access on even address
WE1#	EIM_EB3	GPIO2-31	O	IPU 100K	3,3	Write access on odd address
RD/WR#	EIM_RW	GPIO2-26	O	IPU 100K	3,3	Data direction signal
Miscellaneous						
IRQ1	EIM_A25	GPIO5-2	I	PU 10K	3,3	Interrupt input
IRQ2	EIM_DA15	GPIO3-15	I	PU 10K	3,3	Interrupt input
IRQ3	EIM_CS1	GPIO2-24	I	PU 10K	3,3	Interrupt input
RESI#	RESET_IN_B		I	PU 10K	3,3	Reset input from carrier board
RESO#			O	-	3,3	Reset output to carrier board
BAT			-	-	1,8 – 3,3	Battery backup input for RTC
POWER_ON_BASE[2]			O	-	3,3	Baseboard periphery power on signal
+3V3			-	-	-	+ 3,3V supply
GND			-	-	-	Ground

1: PU/PD depends on the boot configuration. These signals are used as boot configuration pins during reset. During reset these signals shall not be influenced (e.g. by PU/PD or I/O driver) Please ask emtrion for further information.

2: This signal is only supported on DIMM-MX53x-3.

6.2 J3, Extension Connector 1

Name	i.MX53 Pad Name	GPIO	Direction	Add. Wiring at reset	Volt [V]	Description
CSI1 (Video Input Unit 1)						
CSI1_D0	EIM_A17	GPIO2-21	I	PD 10K[1]	3,3	Video image input data
CSI1_D1	EIM_A18	GPIO2-20	I	PU 10K[1]	3,3	Video image input data
CSI1_D2	EIM_A19	GPIO2-19	I	PD 10K[1]	3,3	Video image input data
CSI1_D3	EIM_A20	GPIO2-18	I	PD 10K[1]	3,3	Video image input data

CSI1_D4	EIM_A21	GPIO2-17	I	PD 10K[1]	3,3	Video image input data
CSI1_D5	EIM_A22	GPIO2-16	I	PU 10K[1]	3,3	Video image input data
CSI1_D6	EIM_A23	GPIO6-6	I	IPU 100K	3,3	Video image input data
CSI1_D7	EIM_A24	GPIO5-4	I	IPU 100K	3,3	Video image input data
CSI1_CLK	EIM_A16	GPIO2-22	I	PD 10K[1]	3,3	Video clock input
CSI1_HSYNC	EIM_DA11	GPIO3-11	I	IPU 100K	3,3	Video hsync input
CSI1_VSYNC	EIM_DA12	GPIO3-12	I	IPU 100K	3,3	Video vsync input
LVDS						
DI1_EXT_CLK	EIM_DA13	GPIO3-13	I	IPU 100K	3,3	External Reference clock for LVDS
Miscellaneous						
GND			-	-	-	Ground

1: PU/PD depends on the boot configuration

6.3 J4, Extension Connector 2

Name	i.MX53 Pad Name	GPIO	Direction	Add. Wiring at reset	Volt [V]	Description
LVDS						
LVDS_CLK_P	LVDS_CLK_P		O	-	2,5	P signal of diff. LVDS clock
LVDS_CLK_N	LVDS_CLK_N		O	-	2,5	N signal of diff. LVDS clock
LVDS_TX0_P	LVDS0_TX0_P		O	-	2,5	P signal of diff. LVDS data
LVDS_TX0_N	LVDS0_TX0_N		O	-	2,5	N signal of diff. LVDS data
LVDS_TX1_P	LVDS0_TX1_P		O	-	2,5	P signal of diff. LVDS data
LVDS_TX1_N	LVDS0_TX1_N		O	-	2,5	N signal of diff. LVDS data
LVDS_TX2_P	LVDS0_TX2_P		O	-	2,5	P signal of diff. LVDS data
LVDS_TX2_N	LVDS0_TX2_N		O	-	2,5	N signal of diff. LVDS data
LVDS_TX3_P	LVDS0_TX3_P		O	-	2,5	P signal of diff. LVDS data
LVDS_TX3_N	LVDS0_TX3_N		O	-	2,5	N signal of diff. LVDS data
SATA						
SATA_TXP	SATA_TXP		O	-	2,5	P signal of diff. SATA transmitter
SATA_TXN	SATA_TXM		O	-	2,5	N signal of diff. SATA transmitter
SATA_RXP	SATA_RXP		I	-	2,5	P signal of diff. SATA receiver

SATA_RXN	SATA_RXM		I	-	2,5	N signal of diff. SATA receiver
Keypad						
KPP_COL0	KEY_COL0	GPIO4-6	I/O	IPU 100K	3,3	column signals of keypad
KPP_COL1	KEY_COL1	GPIO4-8	I/O	IPU 100K	3,3	column signals of keypad
KPP_COL2	KEY_COL2	GPIO4-10	I/O	IPU 100K	3,3	column signals of keypad
KPP_COL3	KEY_COL3	GPIO4-12	I/O	IPU 100K	3,3	column signals of keypad
KPP_ROW0	KEY_ROW0	GPIO4-7	I/O	IPD 360K	3,3	row signals of keypad
KPP_ROW1	KEY_ROW1	GPIO4-9	I/O	IPU 100K	3,3	row signals of keypad
KPP_ROW2	KEY_ROW2	GPIO4-11	I/O	IPU 100K	3,3	row signals of keypad
KPP_ROW3	KEY_ROW3	GPIO4-13	I/O	IPU 100K	3,3	row signals of keypad
Miscellaneous						
GND			-	-	-	Ground

6.4 J2, Debugging Connector

Name		Direction	Add. Wiring	Volt [V]	Description
Debug Interface					
TCK	JTAG_TCK	I	PD 10K	2,8	JTAG clock input
TMS	JTAG_TMS	I	IPU 47K	2,8	JTAG mode select input
TRST#	JTAG_TRSTB	I	IPU 47K	2,8	H-UDI reset input
TDI	JTAG_TDI	I	IPU 47K	2,8	Data input
TDO	JTAG_TDO	O	SR 33	2,8	Data output
RTCK		O	PD 10K	2,8	return TCK
JTAG_MODE	JTAG_MOD	I	PD 10K	2,8	
JTAG_DE#		I	PU 10K	2,8	
DBG_ACK		O	PD 10K	2,8	
Miscellaneous					
RESET_IN#	RESET_IN_B	I	PU 10K	2,8	Debugger Reset input
JTAG_RESI#	RESET_IN_B	I	PU 10K	2,8	Manual Reset input
BOOT_MODE0	BOOT_MODE0	I	IPD 100K	2,8	Boot mode selection

BOOT_MODE1	BOOT_MODE1	I	IPD 100K	2,8	Boot mode selection
+3V3		-	-	-	+ 3,3V supply
GND		-	-	-	Ground

7 Technical Characteristics

7.1 Electrical Specifications

Supply voltage	3,3 V, +/-5%
Current consumption	1 A max.

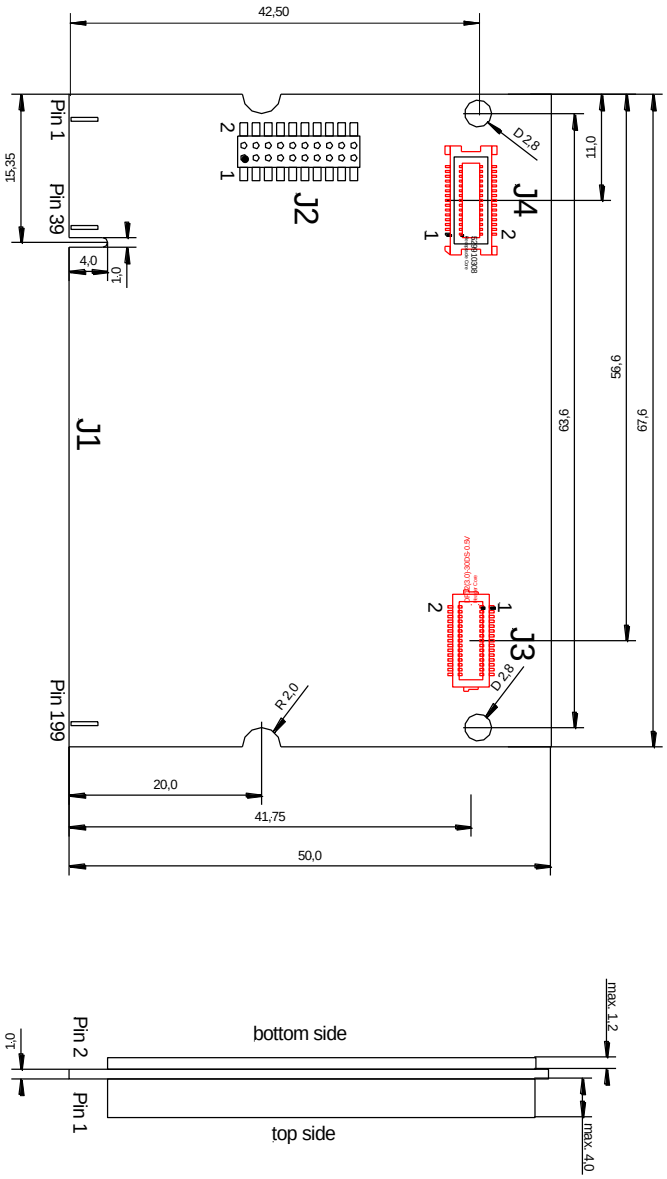
7.2 Environmental Specifications

Operating temperature	
Standard:	0 ... +70°C
Extended:	-40 ... +85°C
Storage temperature	-40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

7.3 Mechanical Specifications

Weight	approx. 15 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 50.0 mm x 10.0 mm

7.3.1 Dimensional Drawing



Red colored parts are located on the bottom side of the CPU module.

8 References

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