emtrion
embedded systems

Product Change Notice - PCN-DIMM-MX53x-3_v02en

Rev	Date/Signature	Changes
1	23.03.2012/Mt	First Revision
2	13.11.2012/Mt	Added Change 5

1 Product affected

Product affected	No.	Rev.	Replacement	Rev.
DIMM-MX53x-2-x/x		R2B	DIMM-MX53x-3-x/x	R3A
DIMM-MX53x-3-x/1G		R3A	DIMM-MX53x-3-x/x	R3B

2 Change 1 – UART1 RTS/CTS

2.1 Key Characteristics of the Change

UART1 RTS and CTS signal switched at the i.MX53x.

2.2 Description of Change to the Customer

The UART1 signals RTS and CTS are switched at the i.MX53x processor. The RTS and CTS signals are now available at the SODIMM connector. The can be used as described.

2.3 Costumer Impact of Change and Recommended Action

UART1 RTS and CTS signals can be used with board revision R3A.

3 Change 2 – Added POWER_ON_BASE signal

3.1 Key Characteristics of the Change

Added the signal POWER_ON_BASE on the SODIMM connector pin 135 and removed the signal 3V3 at that pin.

3.2 Description of Change to the Customer

With that signal the periphery power on the baseboard can be switched on with that signal, if the baseboard supports that feature. More details are described in the Application Note Baseboard Design v003 on the emtrion support homepage.

http://www.support.emtrion.de/doku.php?id=hw:dimmconcept

3.3 Costumer Impact of Change and Recommended Action

If the baseboard supports that feature the periphery power supply is only switched on if the signal POWER_ON_BASE is high.

If the baseboard doesn't support that feature, it has no influence.

4 Change 3 – RAM technology changed from DDR2 SDRAM to DDR3 SDRAM

4.1 Key Characteristics of the Change

The RAM technology is changed from DDR2 SDRAM to DDR3 SDRAM.

4.2 Description of Change to the Customer

The RAM technology is changed from DDR2 SDRAM to DDR3 SDRAM, to support memory space up to 1GB.

4.3 Costumer Impact of Change and Recommended Action

No influence.

5 Change 4 – Added low power mode at VDDGP

5.1 Key Characteristics of the Change

If the i.MX53x core frequency is ≤ 400MHz the VDDGP core voltage can be reduced to save power.

5.2 Description of Change to the Customer

If the i.MX53x core frequency is ≤ 400MHz the VDDGP core voltage can be reduced with the signal LOW_VDDGP_EN. If that signal is set high the core voltage VDDGP is reduced. The signal LOW_VDDGP can be set via the GPIO4-1.

5.3 Costumer Impact of Change and Recommended Action

The test point TP22 is not available any more.

6 Change 5 – 1GB NAND Chip

6.1 Key Characteristics of the Change

The 1GB NAND Chip on the DIMM-MX53x-3 module is replaced.

This change affects only DIMM-MX53x-3 modules with 1GB NAND. The new revision is R3B.

6.2 Description of Change to the Customer

The replacement of the NAND means that the memory structure is changed. The 1GB NAND flashes on the DIMM-MX53x-3 (R3A) modules have a page size of 4kB and one block includes 128 pages.

The 1GB NAND flashes on the DIMM-MX53x-3 (R3B) modules have a page size of 4kB and one block includes 64 pages.

6.3 Costumer Impact of Change and Recommended Action

This issue is valid on for DIMM-MX53x-3 modules with 1GB NAND flash onboard.

Depending on the operating system NAND flash memory structure must be adapted in the SW code.