

# DIMM-RZ/A1H

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## Hardware Manual

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1	08.08.2014/We	First revision
2	04.09.2014/We	LCD-resolution specified

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## 1 Introduction

The DIMM-RZ/A1H processor module is a SODIMM sized CPU board based on the processor RZ/A1H from Renesas. The RZ/A1H includes an ARM single-core Cortex-A9.

The processor cores run up to 384 MHz and includes a variety of functions required for multimedia or industrial applications. These include a 2D graphics accelerator, LCD controller, LVDS interface, camera interface, and a sound input/output module.

This module is equipped with 16MByte QSPI serial-NOR-Flash. The CPU has an internal Ethernet MAC, CAN controller and two USB controllers, which are used as USB Host and USB Device. Additionally a touch controller is available.

All interfaces are accessible through the 200 pin SODIMM edge connector which is mechanically conform with SODIMM memory sockets with 2,5V keying and one additional extension connector.

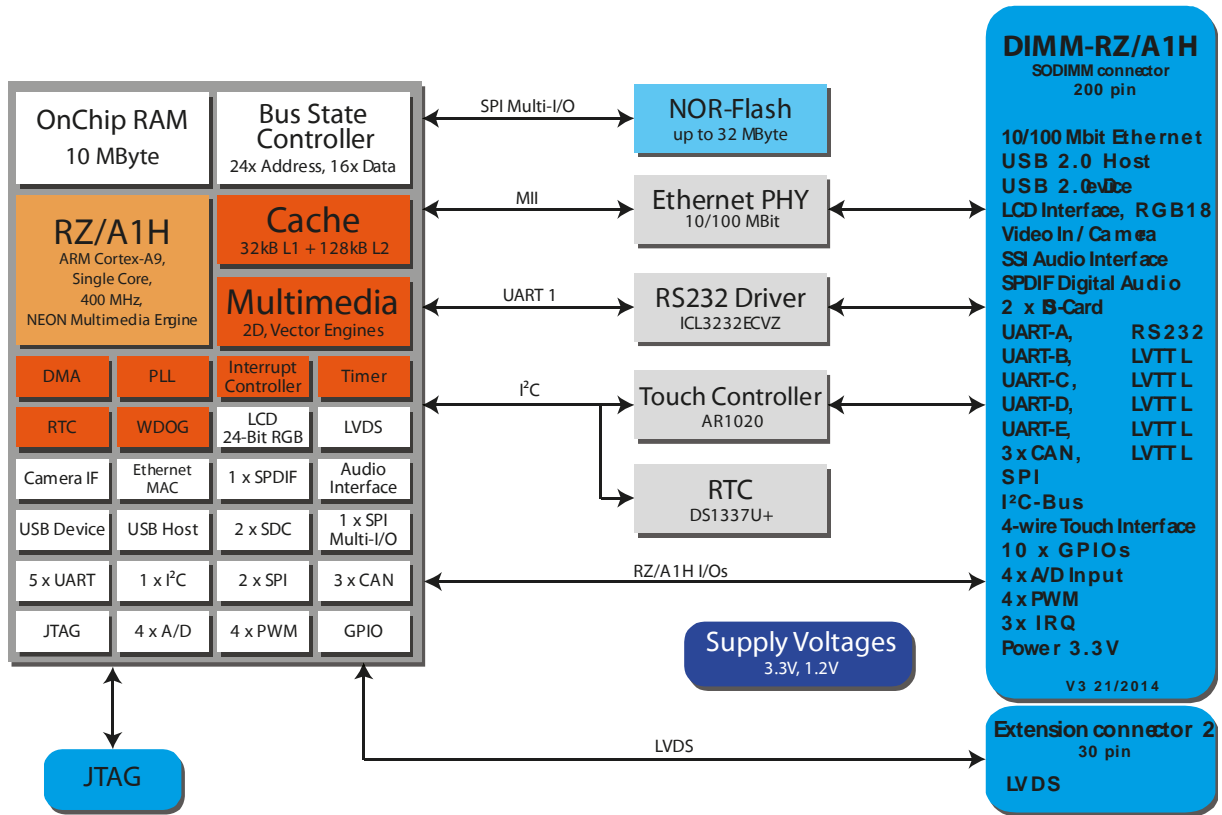
In the following table the features and interfaces of the DIMM-RZ-A1H processor module are described.

DIMM-RZ/A1H
10MB on chip RAM
16MB QSPI serial NOR Flash
1x 10/100Mbit Ethernet
1x USB Host
1x USB Device
1x LCD Interface 16/18/24bit max. WXGA (1280 x 768)
1x 4 wire resistive Touch
1x Video IN 8bit
1x SSI Audio
1x UART RS232
4x UART LVTTTL
1x SPI
2x I2C (one internal, one external)
2x CAN
1x SPDIF in/out
3x IRQ
2x SD Card
1x LVDS 18bit max. max. WXGA (1280 x 768)
min. 8 GPIO
max. 4 PWM

The module is available in the extended temperature range -40°C to 85°C.

## 2 Block Diagram

The following figure shows the block diagram of the DIMM-RZ/A1H.



### 3 Handling Precautions

Please read the following notes prior to installing the DIMM-RZ/A1H processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The DIMM-RZ/A1H does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatically discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

## 4 Functional Description

### 4.1 Processor

The DIMM-RZ/A1H processor module uses the RZ/A1H from Renesas[1]. It includes an ARM single-core Cortex-A9 and runs up to 384 MHz.

In addition to the CPU core with MMU, FPU and Caches, this processor provides features such as:

- Ethernet MAC 10/100Mbit
- USB 2.0 Host with high-speed mode
- USB 2.0 Device with high-speed mode
- 2 SD Card host controllers
- video input module with camera capturing module
- LCD Controller for TFT displays WXGA (1280 x 768) and 16/18/24 bpp
- 18bit LVDS display port up to WXGA (1280 x 768) and 16/18 bpp
- 2D graphic hardware accelerator OpenVG 1.1
- Media processing engine with NEON technology
- CAN controller with five channels
- 5 UARTs with 16 byte FIFO
- I2C bus interfaces
- SPI interfaces
- Watchdog timer
- Real time clock
- Sound interface with I2S format
- Sound interface SPDIF in and out
- Interrupt controller
- 16 and 32-bit timer
- JTAG debug interface

Further details of the processor can be found in the RZ/A1H Hardware User Manual [1].



### 4.1.1 Processor Clocks

The CPU Clock is derived from the 48MHz crystal oscillator which is also used as clock source for the USB-controller. The CPU clock is generated by a fixed divider ( $\times \frac{1}{4}$ ) and a PLL-circuit ( $\times 32$ ) which leads to a maximum CPU-Clock of 384MHz.

All clocks within the processor are derived from this frequency via dividers. The divider for the CPU-clock and of the image-processing clock can be changed by software. All other clock-dividers are fixed.

The internal PLL circuit includes a spread spectrum clock generator (SSCG) which is used to decrease the EMI noise by slightly modulating the output frequency. The SSCG is enabled by default.

More information about the RZ/A1H clock system is described in the chapter Clock Pulse Generator of the RZ/A1H Hardware User Manual [1].

### 4.1.2 Boot Mode

The DIMM-RZ/A1H Uboot can be booted either from the onboard serial Q-SPI NOR-Flash or from a NAND flash memory with the SDC1 controller. The boot mode is configured via the DIP Switch SW1.

SW1-1	SW1-2	Boot source
1 (ON)	0 (OFF)	serial Q-SPI NOR-Flash
0 (OFF)	1 (ON)	SDC1

## 4.2 Serial Q-SPI NOR-Flash

A 16 MByte QSPI serial NOR flash of type S25FL128SDPMFIG11 from Spansion is used as primary boot device.

The integrated RZ/A1H bootloader is configured for booting from the Q-SPI serial NOR flash. Booting from serial NOR flash is enabled if the DIP switch SW1-1 is ON and SW1-2 is OFF.

Besides the Uboot module specific configuration data, like a MAC address, the serial number etc, are also stored in the serial NOR Flash.

## 4.3 Ethernet

The Ethernet interface is realized with the processor internal Media Access Controller (MAC) and an external Physical Layer Interface (PHY) LAN8710Ai from Microchip. The MII interface is used for communication between the MAC and the PHY.

The Ethernet interface supports the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. HP Auto-MDIX is also supported.

The registers of the Ethernet PHY can be configured via the Media Independent Interface (MII).

The Ethernet signal lines (ETH\_TDP, ETH\_TDM, ETH\_RDP, ETH\_RDM) as well as two status signals (SPEED\_LED#, LINK\_LED#) that serve to indicate the link status and the transfer speed are

connected to the SODIMM connector. An appropriate 1:1 transformer with a center tap sourced by 3.3V, must be added externally.

The signal LINK\_LED# indicates if data packages are transferred. ("0" = traffic). The LINK\_LED# signal is an open Drain output signal.

The signal SPEED\_LED# indicates if the data is transferred with 100Mbit/s. ("0" = 100Mbit/s). The LINK\_LED# signal is an open Drain output signal.

A 25MHz crystal is connected to the oscillator input of the Ethernet PHY. The 25MHz clock is used as an input for the internal PLL to generate all needed clocks.

The Ethernet PHY can be reset either by the global reset signal RESO# or by the GPIO-P7-8 of the RZ/A1H. A low at this pin resets the Ethernet PHY.

#### 4.4 USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the internal host controller of the RZ/A1H. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed (1,5Mbps), full-speed (12 Mbps) and high-speed (480Mbps).

To switch the bus power the control line USBH\_PEN# is connected to the SODIMM connector. A logical "0" at the processor GPIO-P6-5 switches the power on; a logical "1" turns the power off. The signal USBH\_OC# reports an overcurrent at the GPIO-P6-10 ("0" = overcurrent).

The data lines and the two control lines are available at the SODIMM connector. A USB power switch must be added externally.

The USBH\_VBUS signal on the SODIMM connector is only a 5V tolerant input to detect the VBUS voltage on the baseboard.

#### 4.5 USB Device

The USB device port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The interface is realized by the internal device controller of the RZ/A1H. The interface is USB 2.0 compliant, supporting data transfers at low-speed (1,5Mbps), full-speed (12 Mbps) and high-speed (480Mbps).

The data lines and the control line USBF\_VBUS are available at the SODIMM connector.

#### 4.6 Graphic Displays

The DIMM-RZ/A1H uses the CPU's video display controller 5 (VDC5) to generate RGB image data for the two display ports. The first is a 24bit TFT display port and the second is a 18bit LVDS display port. Both display ports cannot be used at the same time.

More information about the RZ/A1H Video Display Controller 5 is described in the Hardware User Manual [1]

#### 4.6.1 TFT

The LCD controller of the RZ/A1H can drive TFT displays with resolutions up to WXGA (1280x768) at 16/18/24bpp. The pixel clock for the display data can be generated by the internal clock or via the external LCD0\_EXTCLK. With the external clock individually display timing can be adapted.

All data and control lines are available at the SODIMM connector. The following table describes the function of the data and control lines.

signals	Description
LCD0_D[23:0]	24 colour data; can also be used in 18 or 16 bit mode
LCD0_VSYNC	Vertical synchronization signal
LCD0_HSYNC	horizontal synchronization signal
LCD0_DISP	Data enable signal, if active color data are valid
LCD0_CLK	Display clock
LCD0_EXTCLK	External input clock (e.g. spread spectrum oscillator); can be used by the LCD-controller for the display clock;
LCD0_DON	Display power enable signal; the display backlight power can be switched ("0" backlight off (default); "1" backlight on)
LCD0_VEPWC	Optional display power control output, driven by GPIO-P11-8
LCD0_VCPWC	Optional display power control output, driven by GPIO-P11-9

The following table shows the RGB color mapping on the LCD0\_D[23:0] pins of the SODIMM connector.

SODIMM LCD_D[23:0]	RGB565 (16bit)	RGB666 (18bit)	RGB888 (24bit)
LCD0_D0	B0	B0	B0
LCD0_D1	B1	B1	B1
LCD0_D2	B2	B2	B2
LCD0_D3	B3	B3	B3
LCD0_D4	B4	B4	B4
LCD0_D5	G0	B5	B5
LCD0_D6	G1	G0	B6
LCD0_D7	G2	G1	B7
LCD0_D8	G3	G2	G0
LCD0_D9	G4	G3	G1
LCD0_D10	G5	G4	G2
LCD0_D11	R0	G5	G3
LCD0_D12	R1	R0	G4
LCD0_D13	R2	R1	G5
LCD0_D14	R3	R2	G6
LCD0_D15	R4	R3	G7
LCD0_D16	Fixed to 0	R4	R0
LCD0_D17	Fixed to 0	R5	R1
LCD0_D18	Fixed to 0	Fixed to 0	R2
LCD0_D19	Fixed to 0	Fixed to 0	R3

LCD0_D20	Fixed to 0	Fixed to 0	R4
LCD0_D21	Fixed to 0	Fixed to 0	R5
LCD0_D22	Fixed to 0	Fixed to 0	R6
LC0D_D23	Fixed to 0	Fixed to 0	R7

#### 4.6.2 LVDS

The LCD controller of the RTZ/A1H can drive the LVDS interface with resolutions up to WXGA (1280x768) at 16/18bpp. The pixel clock for the display data can be generated by the internal clock or via the external LCD\_CLK\_IN. With the external clock individually display timings can be adapted.

The LVDS interface uses the RGB signals output from the video display controller 5 and outputs the converted signal. The LVDS lines are available at the extension connector J5. The following table describes the LVDS signals.

Signals	Description
TXCLKOUTP/M	Differential LVDS clock
TXOUT0P/M	First differential LVDS data signal pair
TXOUT1P/M	Second differential LVDS data signal pair
TXOUT2P/M	Third differential LVDS data signal pair

The following table shows the LVDS data format:

signals	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
TXOUT0	LCD_D10	LCD_D23	LCD_D22	LCD_D21	LCD_D20	LCD_D19	LCD_D18
TXOUT1	LCD_D3	LCD_D2	LCD_D15	LCD_D14	LCD_D13	LCD_D12	LCD_D11
TXOUT2	TCON3	TCON0	TCON2	LCD_D7	LCD_D6	LCD_D5	LCD_D4

The following table shows the 18bit colour mapping:

signals	Slot0	Slot1	Slot2	Slot3	Slot4	Slot5	Slot6
TXOUT0	G2	R7	R6	R5	R4	R3	R2
TXOUT1	B3	B2	G7	G6	G5	G4	G3
TXOUT2	DE	VS	HS	B7	B6	B5	B4

#### 4.7 Touch Interface

A 4-wire resistive touch interface is implemented by using the AR1020 touch interface controller from Microchip [2].

The touch controller is connected to the onboard I<sup>2</sup>C bus interface. The IRQ output of the controller is connected to GPIO-P6-11 of the RZ/A1H. A logical high indicates an interrupt.

The 7-bit I<sup>2</sup>C-Address is 0x4D.

The touch interface signals (TOUCH\_XP, TOUCH\_XM, TOUCH\_YP and TOUCH\_YM) are available at the SODIMM connector.

## 4.8 Video Input

The DIMM-RZ/A1H has one Capture Engine Unit (CEU) to fetch external image data from different video sources, such as video codec or CMOS camera modules.

The CEU interface at the DIMM-RZ/A1H is realized with an 8-bit data-bus available at the SODIMM connector. The CEU interface supports various input formats. On some emtrion baseboards the video source can be a video codec or a CMOS camera. To switch between the two video sources the signal VIO\_SRC (GPIO-P3\_6) is available. To reset the video codec on the base board the signal VIO\_RST (GPIO-P3\_5) can be used. Both signals are connected to the SODIMM connector.

The following table describes the CEU signals.

Signals	Description
VIO_D[7:0]	Video input data
VIO_CLK	Video input clock
VIO_HD	Video input horizontal synchronization
VIO_VD	Video input vertical synchronization
VIO_SRC	Video input source selection; "0" = CMOS camera (default); "1" = video codec
VIO_RST#	Video input source reset; "0" = reset; "1" = no reset (default)

## 4.9 Audio Interfaces

### 4.9.1 Audio SSI

The integrated audio module SSI0 of the RZ/A1H can be used to send and receive audio data from external audio codecs. The interface is connected to SODIMM connector, which allows the selection of an external audio codec.

### 4.9.2 Audio SPDIF

The DIMM-RZ/A1H also supports the SPDIF format. The input and output pins at the SODIMM connector have LVTTTL level and will need to be configured external according to the SPDIF specifications.

## 4.10 SD-Card Interface

The RZ/A1H includes two SD Card interfaces (SDC0 and SDC1) to drive memory- or I/O cards. The two interfaces are used for the two 4bit SD Card interfaces of the SODIMM connector. SDC0 of the CPU is used for the interface SDC1 of the SODIMM connector. SDC1 of the CPU is used for SDC2 of the SODIMM.

## 4.11 Serial Ports

The DIMM-RZ/A1H has five serial ports with 16-stage FIFO. All serial ports are integrated in the processor RZ/A1H.

An overview of the UART interfaces is shown as follows:

RZ/A1H interface	SODIMM name	handshake signals	Signal level
UART1	UART_A	-	RS232

UART2	UART_C	-	LVTTTL
UART3	UART_D	-	LVTTTL
UART5	UART_B	CTS, RTS (*)	LVTTTL
UART6	UART_E	-	LVTTTL

(\*) Hand-shake signals CTS and RTS for UART5 are available on the SODIMM pins GPIO0 (CTS5#) and GPIO1 (RTS5#).

UART1 is used as standard debug and communication interface (TERMINAL).

## 4.12 I<sup>2</sup>C- Bus

On the DIMM-RZ/A1H there are two I<sup>2</sup>C bus interfaces (RIIC1 and RIIC3) realized.

The first I<sup>2</sup>C interface (RIIC3) is only routed on the DIMM-RZ/A1H and all onboard I<sup>2</sup>C devices on the module are connected to that interface. The interface works with a transmission speed up to 400 kbps. The interface operates as a master.

Two devices are connected to the RIIC3 bus on DIMM-RZ/A1H:

Slave	Device	Chip Address (7bit)
Real Time Clock	DS1337U+	0x68
Touch controller	AR1020	0x4D

The second I<sup>2</sup>C interface (RIIC1) is routed to the SODIMM connector and can be used exclusive for baseboard functions. The maximum I<sup>2</sup>C speed is 400kb/s.

The external I<sup>2</sup>C interface can be used either in Master mode (default) or in Slave mode. In Slave mode the I<sup>2</sup>C address can be defined in RZ/A1H registers.

The bus connects to the SODIMM connector. The SCL and SDA lines are pulled up with 2,2kΩ resistors to 3,3V, so additional termination is not required.

## 4.13 SPI Interface

The SPI interface SPI4 of the RZ/A1H processor is connected to the SODIMM connector. The four signals SPI\_SCK, SPI\_SS#, SPI\_MOSI and SPI\_MISO are routed to the SODIMM connector.

A second SPI interface SPI1 of the RZ/A1H processor could be available on the SODIMM connector via the pins GPIO6, GPIO7, GPIO8 and GPIO9 (see chapter General Purpose I/Os for more details)

## 4.14 CAN

The RZ/A1H includes a CAN controller with up to five CAN-channels. The implementations of the CAN protocol is conform to the ISO11898-1 specification. The TX and RX signals of the CAN-channel CAN4 are routed to the SODIMM connector.

An additional CAN-channel CAN3 could be used on the SODIMM-connector pins GPIO4 (CAN3RX) and GPIO5 (CAN3TX).

For each CAN interface a CAN transceiver must be realized on the base board. The signal level is 3,3V. The maximum baudrate is 1Mbps.

#### 4.15 General Purpose I/Os

On the DIMM-RZ/A1H are 10 port pins of the processor routed to the SODIMM connector which can be used as GPIOs.

SODIMM Signal	RZ/A1H Port	Direction	PWM	alternative function
GPIO0	GPIO-P6_3	In/Out	Yes	CTS5#
GPIO1	GPIO-P6_4	In/Out		RTS5#
GPIO2	GPIO-P4_0	In/Out	Yes	
GPIO3	GPIO-P4_1	In/Out	Yes	
GPIO4	GPIO-P4_2	In/Out	Yes	CAN3RX
GPIO5	GPIO-P4_3	In/Out	Yes	CAN3TX
GPIO6	GPIO-P11_12	In/Out		SPI1_SCK
GPO7	GPIO-P11_13	In/Out		SPI1_SS
GPO8	GPIO-P11_14	In/Out		SPI1_MOSI
GPO9	GPIO-P11_15	In/Out		SPI1_MISO

The signal level of each GPIO pin is 3,3V.

#### 4.16 PWM

On the DIMM-RZ/A1H two 16bit multi-function timers can be used to generate PWM outputs. In total 5 PWM-outputs are available on the SODIMM if the multiplexed GPIOs are not used.

An overview of the PWM signals is shown as follows:

RZ/A1H Timer channel	RZ/A1H PWM Port	SODIMM GPIO Signal
Channel 2	TIOC2B	GPIO0
Channel 0	TIOC0A	GPIO2
Channel 0	TIOC0B	GPIO3
Channel 0	TIOC0C	GPIO4
Channel 0	TIOC0D	GPIO5

The signal level of each PWM pin is 3,3V.

#### 4.17 DIP Switches, Status LED

Two DIP switches are on the DIMM-RZ/A1H. Via the DIP switches the boot mode of the DIMM-RZ/A1H module can be configured. If a switch is ON the corresponding bit is read as 1. If it is OFF the bit is read as 0. The following table describes the boot mode options.

SW1-1	SW1-2	Boot source
1 (ON)	0 (OFF)	serial Q-SPI NOR-Flash
0 (OFF)	1 (ON)	SDC1

More details of the boot mode options can be found in chapter 3 Boot Mode of in the RZ/A1H Hardware User Manual [1].

A bicolor LED is connected to the port pins GPIO-P8\_11 and GPIO-P8\_12 of the RZ/A1H. If GPIO-P8\_11 is high the green LED is lighting, if GPIO-P8\_12 is high the red LED is lighting.

## 4.18 Interrupts

The processor RZ/A1H has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor.

Generally each GPIO input can be configured as an interrupt input.

On the DIMM-RZ/A1H there are some GPIOs defined as interrupts. The interrupt sources are shown in the following table:

RZ/A1H GPIO Port	Source	polarity	RZ/A1H IRQ
GPIO-P1_10	SODIMM (IRQ_A)	low active	IRQ4
GPIO-P1_11	SODIMM (IRQ_B)	low active	IRQ5
NMI	SODIMM (IRQ_C)	low active	NMI
GPIO-P6_8	RTC (DS1337)	low active	IRQ0
GPIO-P6_11	Touch (AR1020)	high active	IRQ3

IRQ\_A, IRQ\_B and IRQ\_C are general purpose interrupts from the SODIMM connector. The signal level of each interrupt is 3,3V.

The RTC interrupt can be asserted by the onboard RTC chip.

The Touch interrupt can be asserted by the onboard Touch controller chip.

## 4.19 Reset

There are several ways for issuing a reset signal:

- Two voltage monitor checks the board voltages. If one voltage is out of tolerance a module reset is asserted. The reset time in that case is min 125ms.
- The active low signal RESI# at the SODIMM connector and the signal JTAG\_RESI# at the debug connector, can assert a reset.
- If enabled the Watch-dog timer of the RZ/A1H can generate a module reset signal by asserting WDTOVF# pin to low.
- The processor can take control of the WDTOVF# via GPIO-P3\_7. By setting GPIO-P3\_7 to low a SW-reset can be generated which will generate a module reset.

All resets are hardware resets of the whole board. The duration of the reset signal is min. 125ms. For resetting external devices the reset signal is available as an output (RESO#) at the SODIMM connector.



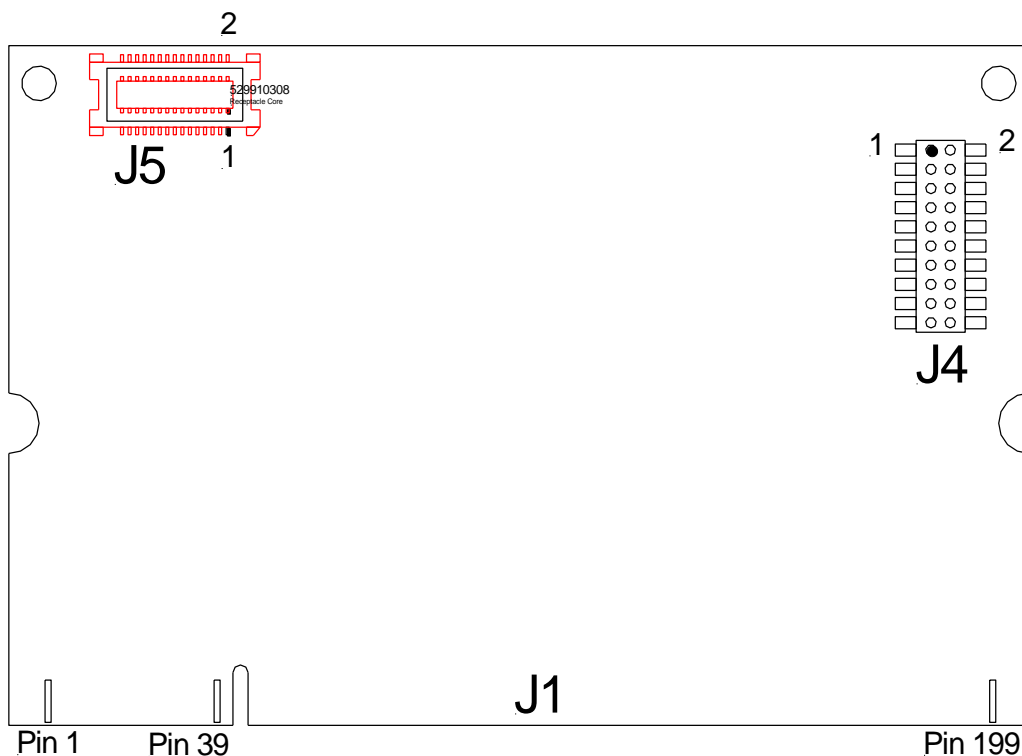
## 4.20 Power Supply

The typical power consumption is 400mA (tbc) at +3,3V, which must be supplied via the SODIMM connector. The onboard required voltages for the processor and the other parts are generated on board via DC/DC-converters.

The SODIMM BAT pin is the battery input pin for the RTC power supply. The typical power consumption of the RTC via the BAT pin is < 1µA.

## 4.21 Connectors

On the DIMM-RZ/A1H there are 3 connectors. J1 is the main SODIMM connector. J4 is the JTAG debug connector. J5 is the extension connector 2 for LVDS.



Red colored parts are located on the bottom side of the CPU module.

### 4.21.1 DIMM Interface

Most interface signals of the board are available at the SODIMM connector.

The DIMM interface is a 200 pos SODIMM connector that fits mechanically into a regular DDR1 SODIMM memory socket with 2,5V keying. These sockets are available from various manufacturers.

Usage details of the connector and its electrical and mechanical characteristics can be found further down in this document.

#### Notes:

The pin out of the SODIMM connector is NOT compatible with memory sockets. Insertion into a socket with wrong pin out may damage the DIMM-RZ/A1H and the carrier board.

Most of the pins are directly connected with the processor RZ/A1H.

#### **4.21.2 Debugging interface**

At the 20 pole pin-header J5 all signals of the ARM debug interface are available.

Please contact emtrion GmbH for further details how to connect an emulator to J5.

#### **4.21.3 Extension Interface**

The interface LVDS is routed to the extension connector J5. More details about the pin assignment and the connector type are described in chapter 5.2. The signal characteristics are described in chapter 6.2.

## 5 Pin Assignments

### 5.1 J1, SODIMM

Type SODIMM, 200 pos, 2,5V keying

Pin	Signal	Interface		Signal	Pin	
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2	
3	ETH_TDP			USBH_OC#	4	
5	ETH_TDM			USBH_DM	6	
7	GND			USBH_DP	8	
9	ETH_RDP			USB Device	USBF_VBUS	10
11	ETH_RDM				USBF_DM	12
13	LINK_LED#		USBF_DP		14	
15	n/c		USB Host	Power	GND	16
17	CAN4_TX		CAN	UART-A	UART1_TXD#	18
19	CAN4_RX	UART1_RXD#			20	
21	UART6_TXD	UART-E	n/c		22	
23	UART6_RXD		n/c		24	
25	UART3_TXD	UART-D	Touch		Touch_XP	26
27	UART3_RXD	UART-C		Touch_XM	28	
29	UART2_TXD			Touch_YP	30	
31	UART2_RXD	UART-B	A/D	Touch_YM	32	
33	UART5_TXD			AN1	34	
35	UART5_RXD			AN5	36	
37	AN7	A/D	AN6	38		
39	+3V3	Power		GND	40	
41	LCD0_D22	LCD		LCD0_D23	42	
43	LCD0_D20			LCD0_D21	44	
45	LCD0_D18			LCD0_D19	46	
47	LCD0_D16			LCD0_D17	48	
49	LCD0_D14			LCD0_D15	50	
51	LCD0_D12			LCD0_D13	52	

53	LCD0_D10		LCD0_D11	54	
55	LCD0_D8		LCD0_D9	56	
57	LCD0_D6		LCD0_D7	58	
59	LCD0_D4		LCD0_D5	60	
61	LCD0_D2		LCD0_D3	62	
63	LCD0_D0		LCD0_D1	64	
65	+3V3	<b>Power</b>		GND	66
67	n/c	<b>LCD</b>		LCD0_EXTCLK	68
69	LCD0_DISP			LCD0_CLK	70
71	LCD0_HSYN			LCD0_DON	72
73	LCD0_VSYN			LCD0_VCPWC*	74
75	n/c			LCD0_VEPWC*	76
77	VOU_RST#*	<b>CSI1</b>		VIO_D7	78
79	VIO_FLD			VIO_D6	80
81	n/c			VIO_D5	82
83	VIO_CLK			VIO_D4	84
85	VIO_HD			VIO_D3	86
87	VIO_VD			VIO_D2	88
89	VIO_SRC			VIO_D1	90
91	VIO_RST#	VIO_D0	92		
93	+3V3	<b>Power</b>		GND	94
95	SD_D0_1	<b>SDC2</b>		SD_D0_0	96
97	SD_D1_1			SD_D1_0	98
99	SD_D2_1			SD_D2_0	100
101	SD_D3_1			SD_D3_0	102
103	SD_CMD_1			SD_CMD_0	104
105	SD_CLK_1			SD_CLK_0	106
107	SD_CD_1#			SD_CD_0#	108
109	SD_WP_1	SD_WP_0	110		
111	SPI4_SS#	<b>SPI</b>		SPI4_MISO	112
113	SPI4_SCK			SPI4_MOSI	114

<b>115</b>	RIIC1SCL	<b>I2C</b>	<b>Audio</b>	SSISCK0	<b>116</b>
<b>117</b>	RIIC1SDA			SSIWS0	<b>118</b>
<b>119</b>	SPDIF_IN	<b>SPDIF</b>		SSIRXD0	<b>120</b>
<b>121</b>	SPDIF_OUT			SSITXD0	<b>122</b>
<b>123</b>	GND	<b>Power</b>		n/c	<b>124</b>
<b>125</b>	GPIO8/SPI1_MOSI	<b>GPIO</b>		GPIO9/MISO	<b>126</b>
<b>127</b>	GPIO6/SPI_SCK		GPO7/SPI_SS	<b>128</b>	
<b>129</b>	GPIO4/CAN3RX		GPIO5/CAN3TX	<b>130</b>	
<b>131</b>	GPIO2		GPIO3	<b>132</b>	
<b>133</b>	GPIO0/CTS5#		GPIO1/RTS5#	<b>134</b>	
<b>135</b>	+3V3	<b>Power</b>	GND	<b>136</b>	
<b>137</b>	n/c	<b>Address A[23:0]</b>	n/c	<b>138</b>	
<b>139</b>	n/c		n/c	<b>140</b>	
<b>141</b>	n/c		n/c	<b>142</b>	
<b>143</b>	n/c		n/c	<b>144</b>	
<b>145</b>	n/c		n/c	<b>146</b>	
<b>147</b>	n/c		n/c	<b>148</b>	
<b>149</b>	n/c		n/c	<b>150</b>	
<b>151</b>	n/c		n/c	<b>152</b>	
<b>153</b>	n/c		n/c	<b>154</b>	
<b>155</b>	n/c		n/c	<b>156</b>	
<b>157</b>	n/c		n/c	<b>158</b>	
<b>159</b>	n/c		n/c	<b>160</b>	
<b>161</b>	+3V3	<b>Power</b>	GND	<b>162</b>	
<b>163</b>	n/c	<b>Data D[15:0]</b>	n/c	<b>164</b>	
<b>165</b>	n/c		n/c	<b>166</b>	
<b>167</b>	n/c		n/c	<b>168</b>	
<b>169</b>	n/c		n/c	<b>170</b>	
<b>171</b>	n/c		n/c	<b>172</b>	
<b>173</b>	n/c		n/c	<b>174</b>	
<b>175</b>	n/c	n/c	<b>176</b>		

<b>177</b>	n/c		n/c	<b>178</b>	
<b>179</b>	reserved**	<b>Bus Control</b>	n/c	<b>180</b>	
<b>181</b>	reserved**		reserved**	<b>182</b>	
<b>183</b>	reserved**		IRQ1#	<b>184</b>	
<b>185</b>	reserved**		IRQ2#	<b>186</b>	
<b>187</b>	reserved**		IRQ3#	<b>188</b>	
<b>189</b>	reserved**		RESO#	<b>190</b>	
<b>191</b>	reserved**		RESI#	<b>192</b>	
<b>193</b>	reserved**		reserved**	<b>194</b>	
<b>195</b>	n/c		reserved**	<b>196</b>	
<b>197</b>	reserved**		reserved**	<b>198</b>	
<b>199</b>	BAT		<b>Power</b>	GND	<b>200</b>

\* These signals are not available by default. Please ask emtrion for further information.

\*\* These have no function on the DIMM-RZ/A1H. They are pulled-down or pulled up.

## 5.2 J5, Extension Connector 2

Type 30-pin connector, Molex 529910308 (Receptacle)  
 Corresponding header for base boards: Molex 537480308

### 5.2.1 Standard CPU Modules

Pin	Signal	Pin	Signal
1	n/c	2	TXOUT2M
3	n/c	4	TXOUT2P
5	n/c	6	TXOUT0M
7	n/c	8	TXOUT0P
9	GND	10	GND
11	n/c	12	TXOUT1M
13	n/c	14	TXOUT1P
15	n/c	16	GND
17	n/c	18	TXCLKOUTM
19	n/c	20	TXCLKOUTP
21	n/c	22	GND
23	n/c	24	n/c
25	n/c	26	n/c
27	n/c	28	GND
29	n/c	30	n/c

### 5.3 J4, Debugging Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	RTCK*	2	TCK
3	GND	4	GND
5	+3V3	6	TRST#
7	+3V3	8	+3V3
9	GPIO_JTAG	10	TDO
11	n/c	12	JTAG_DE#**
13	n/c	14	TMS
15	n/c	16	TDI
17	GND	18	DBG_ACK*
19	RESET_BTN#	20	JTAG_RST#

\* These pin have no function on DIMM-RZ/A1H. It is pulled-down.

\*\* These pin have no function on DIMM-RZ/A1H. It is pulled-up.



## 6 Signal Characteristics

Abbreviations:

AI analogue input  
 AO analogue output  
 A I/O analogue bidirectional  
 I digital input  
 O digital output  
 I/O digital bidirectional  
 O(OD) digital open drain output

PU xK x K $\Omega$  pullup resistor  
 PD xK x K $\Omega$  pulldown resistor  
 SR xR x  $\Omega$  series resistor

### 6.1 J1, SODIMM Connector

Name	RZ/A1H Pin Name	Direction	Add. Wiring at Reset	Volt	Max. Current	Description
<b>Ethernet</b>						
SPEED_LED#		O(OD)	-	3,3V	20mA	100 Mbit indicator
ETH_TDP		AO	PU 49R9	-	N/A	TX diff. output pos.
ETH_TDM		AO	PU 49R9	-	N/A	TX diff. output neg.
ETH_RDP		AI	PU 49R9	-	N/A	RX diff. input pos.
ETH_RDN		AI	PU 49R9	-	N/A	RX diff. input neg.
LINK_LED#		O(OD)	-	3,3V	20mA	traffic indicator
<b>USB Host</b>						
USBH_PEN#	P6_5	O	PU 10K	3,3V		USB power enable signal for power switch
USBH_OC#	P6_10	I	PU 10K	3,3V		USB overcurrent signal from power switch

USBH_DP	DP1	I/O	-	3,0V	N/A	Diff. data positive
USBH_DM	DM1	I/O	-	3,0V	N/A	Diff. data negative
<b>USB Device</b>						
USBF_VBUS	VBUSIN0	I	-	5V	N/A	VBUS detection
USBF_DP	DP0	I/O	-	3,0V	N/A	Diff. data positive
USBF_DM	DM0	I/O	-	3,0V	N/A	Diff. data negative
<b>UART</b>						
UART1_TXD#	P6_12	O	-	RS232	2mA	RS232 transmit data
UART1_RXD#	P6_13	I	-	RS232	N/A	RS232 receive data
UART2_TXD	P8_6	O	PU 10K	3,3V	2mA	transmit data
UART2_RXD	P8_4	I	PU 10K	3,3V	N/A	receive data
UART3_TXD	P6_1	O	PU 10K	3,3V	2mA	transmit data
UART3_RXD	P6_0	I	PU 10K	3,3V	N/A	receive data
UART5_TXD	P6_6	O	PU 10K	3,3V	2mA	transmit data
UART5_RXD	P6_7	I	PU 10K	3,3V	N/A	receive data
UART6_TXD	P6_14	O	PU 10K	3,3V	2mA	transmit data
UART6_RXD	P6_15	I	PU 10K	3,3V	N/A	receive data
<b>CAN</b>						
CAN4_TX	P8_10	O	-	3,3V	2mA	transmit data
CAN4_RX	P2_14	I	PU 10K	3,3V	N/A	receive data
<b>4-Wire Resestive Touch interface</b>						
TOUCH_XP		A I/O	-	3,3V	N/A	X plus terminal
TOUCH_XM		A I/O	-	3,3V	N/A	X minus terminal
TOUCH_YP		A I/O	-	3,3V	N/A	Y plus terminal
TOUCH_YM		A I/O	-	3,3V	N/A	Y minus terminal
<b>LCD (Graphic Display)</b>						
LCD0_DON	P6_9	O	-	3,3V	2mA	LCD display enable signal (Backlight)
LCD0_DISP	P3_4	O	-	3,3V	2mA	LCD data enable signal

LCD0_VSYNC	P3_2	O	-	3,3V	2mA	LCD frame sync output
LCD0_HSYNC	P3_1	O	-	3,3V	2mA	LCD line sync output
LCD0_D0	P11_7	O	-	3,3V	2mA	LCD colour data
LCD0_D1	P11_6	O	-	3,3V	2mA	LCD colour data
LCD0_D2	P11_5	O	-	3,3V	2mA	LCD colour data
LCD0_D3	P11_4	O	-	3,3V	2mA	LCD colour data
LCD0_D4	P11_3	O	-	3,3V	2mA	LCD colour data
LCD0_D5	P11_2	O	-	3,3V	2mA	LCD colour data
LCD0_D6	P11_1	O	-	3,3V	2mA	LCD colour data
LCD0_D7	P11_0	O	-	3,3V	2mA	LCD colour data
LCD0_D8	P10_15	O	-	3,3V	2mA	LCD colour data
LCD0_D9	P10_14	O	-	3,3V	2mA	LCD colour data
LCD0_D10	P10_13	O	-	3,3V	2mA	LCD colour data
LCD0_D11	P10_12	O	-	3,3V	2mA	LCD colour data
LCD0_D12	P10_11	O	-	3,3V	2mA	LCD colour data
LCD0_D13	P10_10	O	-	3,3V	2mA	LCD colour data
LCD0_D14	P10_9	O	-	3,3V	2mA	LCD colour data
LCD0_D15	P10_8	O	-	3,3V	2mA	LCD colour data
LCD0_D16	P10_7	O	-	3,3V	2mA	LCD colour data
LCD0_D17	P10_6	O	-	3,3V	2mA	LCD colour data
LCD0_D18	P10_5	O	-	3,3V	2mA	LCD colour data
LCD0_D19	P10_4	O	-	3,3V	2mA	LCD colour data
LCD0_D20	P10_3	O	-	3,3V	2mA	LCD colour data
LCD0_D21	P10_2	O	-	3,3V	2mA	LCD colour data
LCD0_D22	P10_1	O	-	3,3V	2mA	LCD colour data
LCD0_D23	P10_0	O	-	3,3V	2mA	LCD colour data
LCD0_CLK	P3_0	O	-	3,3V	2mA	LCD data clock
LCD0_EXTCLK	P5_8	I	PU 10K	3,3V	N/A	External Reference clock for LCD
LCD0_VCPWC	P11_8	O	-	3,3V	2mA	Reserved LCD signal, can be used as GPIO

LCD0_VEPWC	P11_9	O	-	3,3V	2mA	Reserved LCD signal, can be used as GPIO
VOU_RST#	P11_10	O	Out(LOW)/PD 10k	3,3V	2mA	Reserved LCD signal, can be used as GPIO
<b>CSI1 (Video Input Unit 1)</b>						
VIO_D0	P2_0	I	-	3,3V	N/A	Video image input data
VIO_D1	P2_1	I	-	3,3V	N/A	Video image input data
VIO_D2	P2_2	I	-	3,3V	N/A	Video image input data
VIO_D3	P2_3	I	-	3,3V	N/A	Video image input data
VIO_D4	P2_4	I	-	3,3V	N/A	Video image input data
VIO_D5	P2_5	I	-	3,3V	N/A	Video image input data
VIO_D6	P2_6	I	-	3,3V	N/A	Video image input data
VIO_D7	P2_7	I	-	3,3V	N/A	Video image input data
VIO_CLK	P1_5	I	-	3,3V	N/A	Video clock input
VIO_HD	P1_1	I	-	3,3V	N/A	Video hsync input
VIO_VD	P1_0	I	-	3,3V	N/A	Video vsync input
VIO_SRC	P3_6	O	PD 10K	3,3V	2mA	Selection of either camera or video codec input
VIO_RST#	P3_5	O	PD 10K	3,3V	2mA	Reset signal for video device
<b>SPI</b>						
SPI_SS#	P2_9	O	PU 10K	3,3V	2mA	Slave select output
SPI_SCK	P2_8	O	-	3,3V	2mA	Clock output
SPI_MISO	P2_11	I	-	3,3V	N/A	Input data from slave
SPI_MOSI	P2_10	O	-	3,3V	2mA	Output data to slave
<b>SD Card Interface</b>						
SD_D0_0	P4_11	I/O	PU 22K	3,3V	2mA	SDC data
SD_D1_0	P4_10	I/O	PU 22K	3,3V	2mA	SDC data
SD_D2_0	P4_15	I/O	PU 22K	3,3V	2mA	SDC data
SD_D3_0	P4_14	I/O	PU 22K	3,3V	2mA	SDC data
SD_CMD_0	P4_13	I/O	PU 22K/SR 22R	3,3V	2mA	CMD signal
SD_CLK_0	P4_12	O	SR 22R	3,3V	2mA	SDC Clock output
SD_CD_0#	P4_8	I	PU 22K	3,3V	N/A	Card detect input

SD_WP_0	P4_9	I	PU 22K	3,3V	N/A	Write protect input
SD_D0_1	P3_11	I/O	PU 22K	3,3V	2mA	SDC data
SD_D1_1	P3_10	I/O	PU 22K	3,3V	2mA	SDC data
SD_D2_1	P3_15	I/O	PU 22K	3,3V	2mA	SDC data
SD_D3_1	P3_14	I/O	PU 22K	3,3V	2mA	SDC data
SD_CMD_1	P3_13	I/O	PU 22K/SR 22R	3,3V	2mA	CMD signal
SD_CLK_1	P3_12	O	SR 22R	3,3V	2mA	SDC Clock output
SD_CD_1#	P3_8	I	PU 22K	3,3V	N/A	Card detect input
SD_WP_1	P3_9	I	PU 22K	3,3V	N/A	Write protect input
<b>I2C</b>						
RI2C1_SCL	P1_6	I/O	PU 2K2	3,3V	2mA	I <sup>2</sup> C clock signal
RI2C1_SDA	P1_7	I/O (OD)	PU 2K2	3,3V	2mA	I <sup>2</sup> C data signal
<b>Audio SSI</b>						
SSISCK0	P4_4	I/O	IPU 100K	3,3V	2mA	Sound bit clock
SSIWS0	P4_5	I	IPU 100K	3,3V	N/A	Sound L/R signal
SSIRXD0	P4_6	I	IPU 100K	3,3V	N/A	Sound serial input data
SSITXD0	P4_7	O	IPU 100K	3,3V	2mA	Sound serial output data
<b>Audio SPDIF</b>						
SPDIF_IN	P8_8	I	PU 47K	3,3V	N/A	SPDIF sound serial input data
SPDIF_OUT	P8_9	O	-	3,3V	2mA	SPDIF Sound serial output data
<b>General Purpose I/O</b>						
GPIO0	P6_3	I/O	-	3,3V	2mA	digital input / output
GPIO1	P6_4	I/O	-	3,3V	2mA	digital input / output
GPIO2	P4_0	I/O	-	3,3V	2mA	digital input / output
GPIO3	P4_1	I/O	-	3,3V	2mA	digital input / output
GPIO4	P4_2	I/O	-	3,3V	2mA	digital input / output
GPIO5	P4_3	I/O	-	3,3V	2mA	digital input / output
GPIO6	P11_12	I/O	-	3,3V	2mA	digital input / output
GPIO7	P11_13	I/O	-	3,3V	2mA	digital output only

GPIO8	P11_14	I/O	-	3,3V	2mA	digital input / output
GPIO9	P11_15	I/O	-	3,3V	2mA	digital input / output
<b>Miscellaneous</b>						
IRQ_A	P1_10	I	PU 1K	3,3V	N/A	Interrupt input
IRQ_B	P1_11	I	PU 1K	3,3V	N/A	Interrupt input
IRQ_C	NMI	I	PU 1K	3,3V	N/A	Interrupt input
RESI#	RES#	I	PU 1K	3,3V	N/A	Reset input from carrier board
RESO#		O	-	3,3V	2mA	Reset output to carrier board
BAT		-	-	2,3V - 3,3V	N/A	Battery backup input for RTC
+3V3		-	-	-	N/A	+ 3,3V supply
GND		-	-	-	N/A	Ground

## 6.2 J5, Extension Connector 2

### 6.2.1 Standard CPU Modules

Name	RZ/A1H Pin Name	Direction	Add. Wiring at reset	Volt	Max. Current	Description
TXCLKOUTP		O	-	1,25V	2mA	P signal of diff. LVDS clock
TXCLKOUTM		O	-	1,25V	2mA	N signal of diff. LVDS clock
TXOUT0P		O	-	1,25V	2mA	P signal of diff. LVDS data
TXOUT0M		O	-	1,25V	2mA	N signal of diff. LVDS data
TXOUT1P		O	-	1,25V	2mA	P signal of diff. LVDS data
TXOUT1M		O	-	1,25V	2mA	N signal of diff. LVDS data
TXOUT2P		O	-	1,25V	2mA	P signal of diff. LVDS data
TXOUT2M		O	-	1,25V	2mA	N signal of diff. LVDS data
GND		-	-	-	N/A	Ground

### 6.3 J4, Debugging Connector

Name	RZ/A1H Pad Name	Direction	Add. Wiring	Volt	Max. Current	Description
<b>Debug Interface</b>						
TCK	TCK	I	PD 10K	3,3V	N/A	JTAG clock input
TMS	TMS	I	PU 10K	3,3V	N/A	JTAG mode select input
TRST#	TRST#	I	PU 10K	3,3V	N/A	reset input of JTAG port
TDI	TDI	I	PU 10K	3,3V	N/A	JTAG Data input
TDO	TDO	O		3,3V	1mA	JTAG Data output
RTCK		O	PD 10K	3,3V	N/A	return TCK
JTAG_DE#		I	PU 10K	3,3V	N/A	Reserved, pulled up
DBG_ACK		O	PD 10K	3,3V	N/A	Reserved, pulled down
<b>Miscellaneous</b>						
JTAG_RESET#	RES#	I/O (OD)	PU 10K	3,3V	2mA	Debugger Reset input/output
RESET_BTN#	RES#	I	PU 1K	3,3V	2mA	Manual Reset input
+3V3		-	-	-	N/A	+ 3,3V supply
GND		-	-	-	N/A	Ground



## 7 Technical Characteristics

### 7.1 Electrical Specifications

<b>Supply voltage</b>	3,3 V, +/-5%
<b>Current consumption</b>	up to 400mA, depending on CPU and GPU load (tbd)

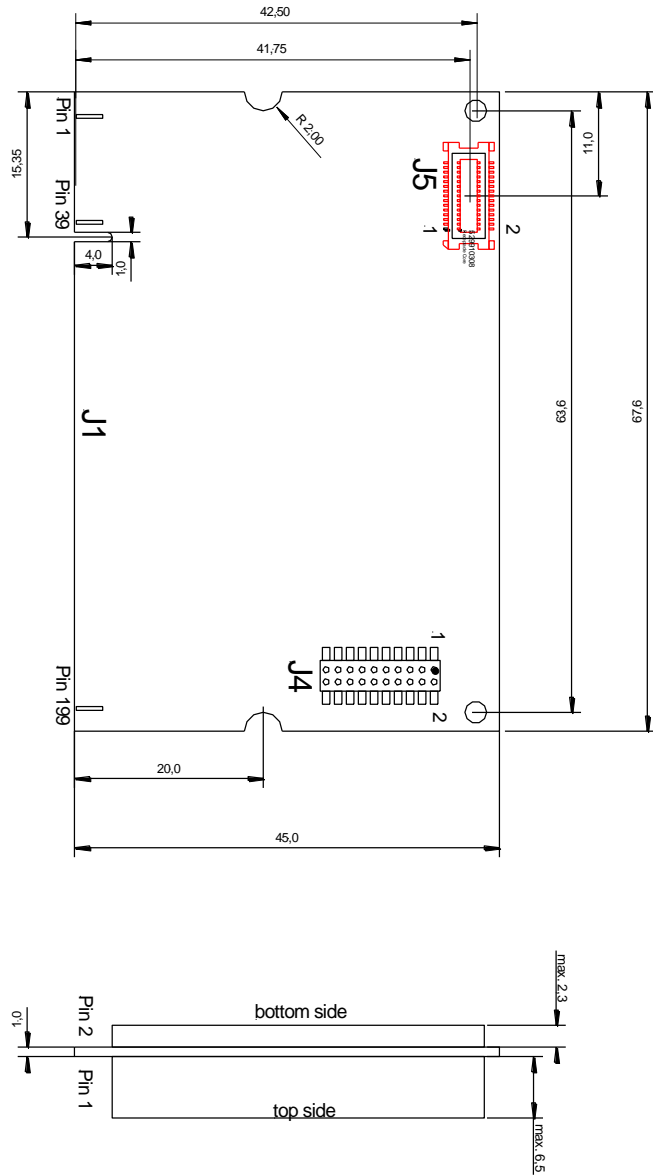
### 7.2 Environmental Specifications

<b>Operating temperature</b>	
Extended:	-40 ... +85°C
<b>Storage temperature</b>	-40 ... +125°C
<b>Relative humidity</b>	0 ... 95 %, non-condensing

### 7.3 Mechanical Specifications

<b>Weight</b>	approx. 17 g
<b>Board</b>	Glasepoxi FR-4, UL-listed, 6 layers
<b>Dimensions</b>	67.6 mm x 45.0 mm x 10.0 mm

## 8 Dimensional Drawing



Red colored parts are located on the bottom side of the CPU module.

## 9 References

- [1] RZ/A1H  
User Manual: Hardware  
Renesas Microprocessor RZ Family / RZ/A Series  
Rev.1.00 Jun 2014  
Renesas Electronics
  
- [2] AR1020  
Datasheet  
AR1000 Series Resistive Touch Screen Controller  
DS41393A  
Microchip Technology Inc.