

# DIMM-Eco-Base Cadun

HiCO.DIMM compliant baseboard

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## Hardware Description

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Rev	Date/Signature	Changes
1	03.04.2013/Sr	First revision
2	03.07.2014/Ko	Pin Information of microSD and Audio Jack added
3	10.02.2015/We	Designators of microSD-connector (J8) and I/O extension connector (J12) corrected in chapter 7.

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## 1 Introduction

DIMM-Eco-Base Cadun is an advancement of the DIMM-Eco-Base Verno to support Core modules with high power consumption like the DIMM-MX6. Also a LVDS interface is added to provide three display interfaces. The board currently supports several Core modules: DIMM-SH7723, DIMM-SH7724, DIMM-EMEV2, DIMM-MX257, DIMM-MX53x, DIMM-AM335x and DIMM-MX6x.

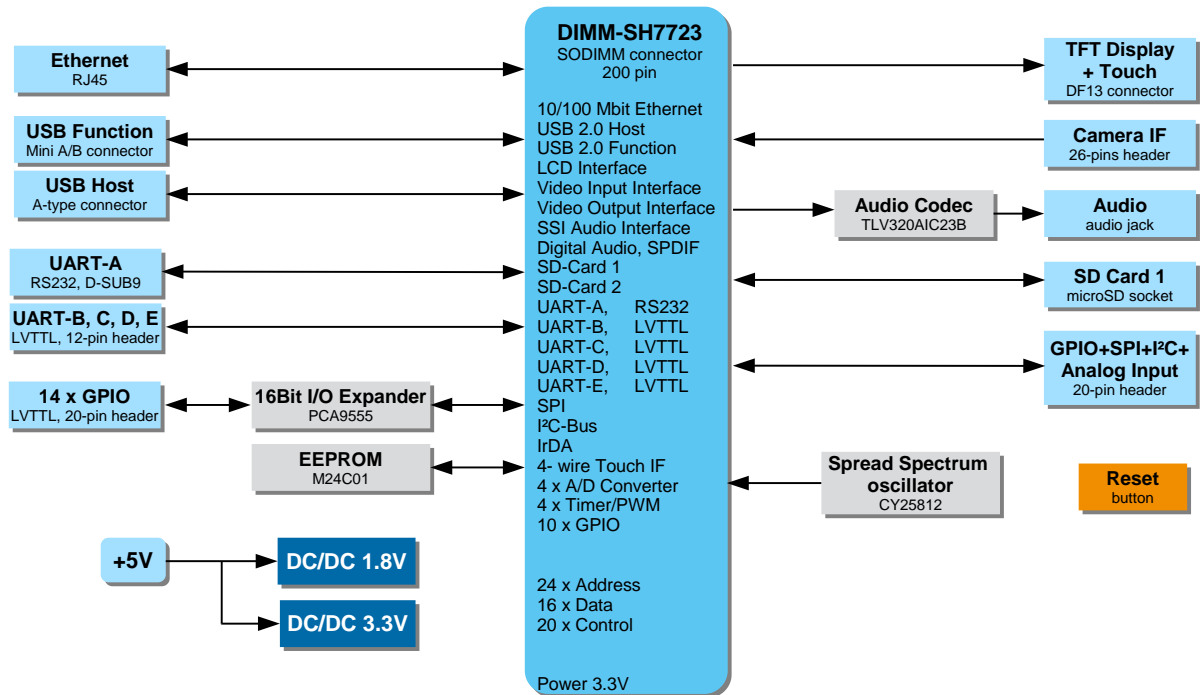
DIMM-Eco-Base Cadun is intended to be used as a development platform and demonstrates the capabilities of the emtrion Core modules, as well as the advantages of the DIMM interface. Or it can be used in series products. Cadun provides the important connectors that are needed to make a useful use of the Core module's features.

This Hardware manual describes the physical and electrical characteristics of the board. It covers the use of Cadun with all supported Core modules but only gives additional details that are specific to the base. For this reason, it has to be used together with the manuals of the Core.

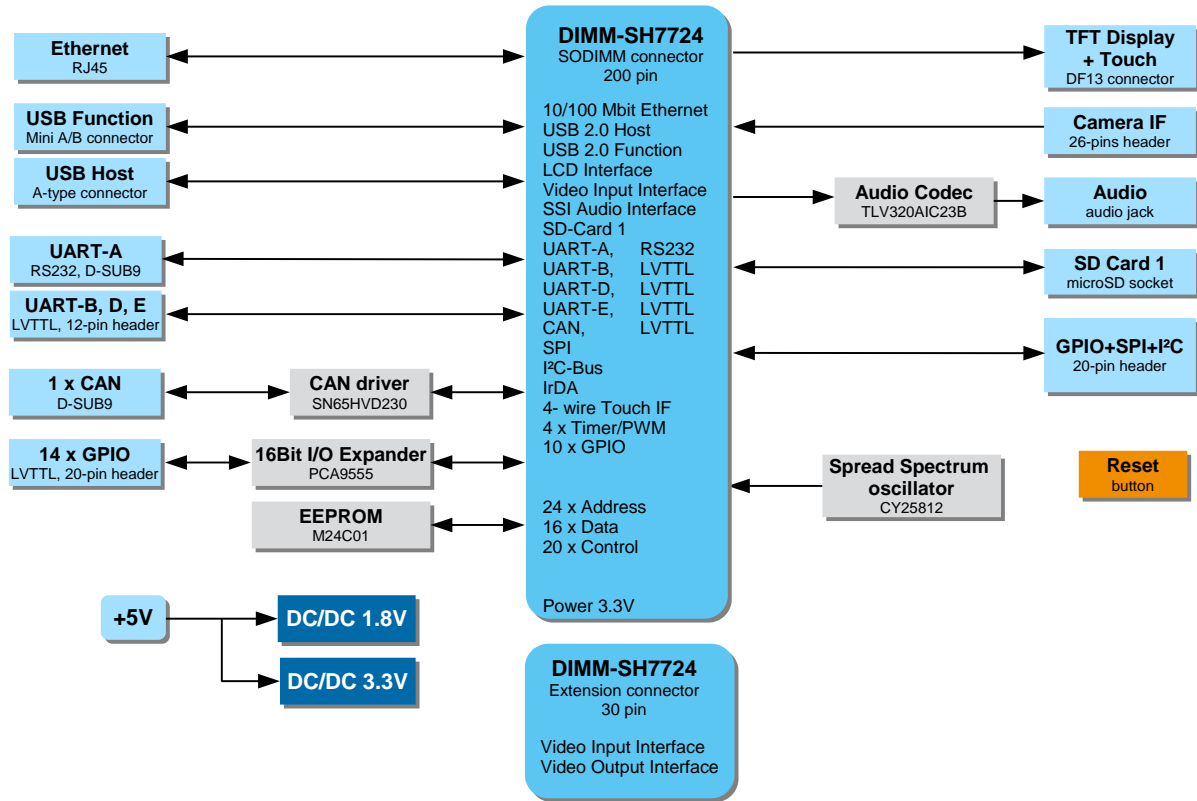
Most interfaces of the Cadun base board are common to all Core modules. Relevant differences between these boards are explicitly mentioned in this manual.

## 2 Block Diagram

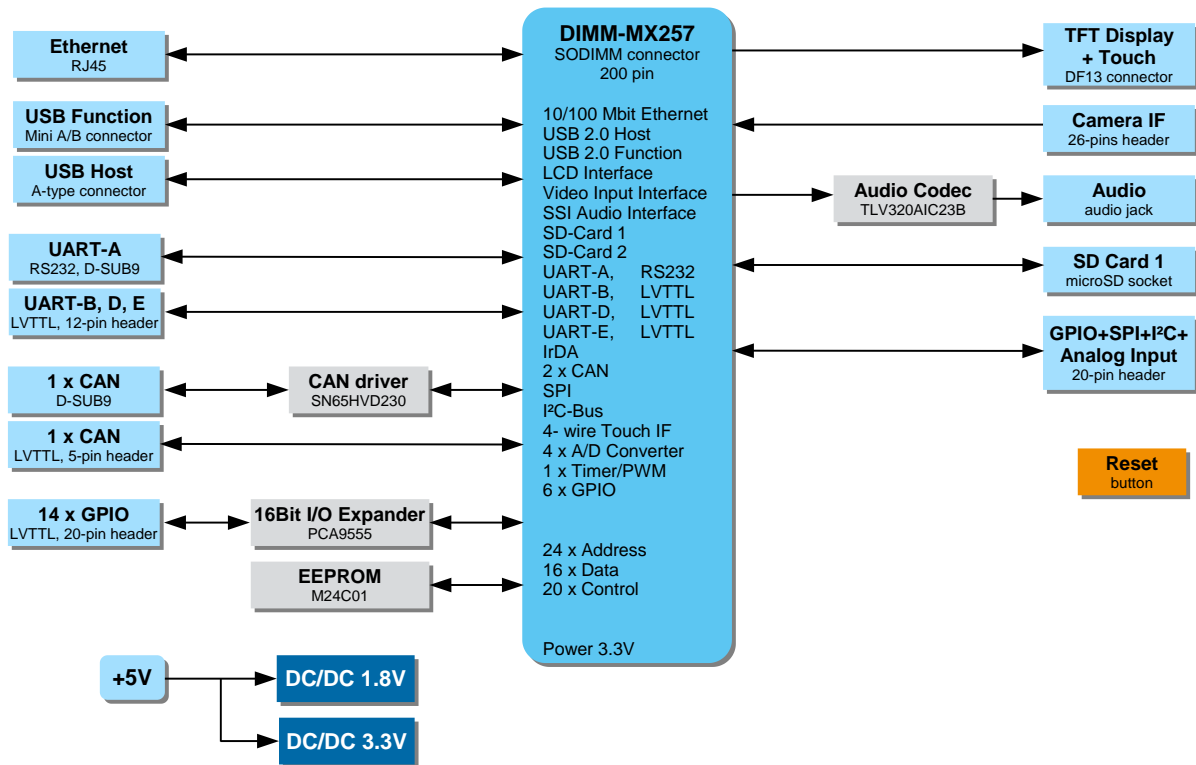
### 2.1 DIMM-SH7723



## 2.2 DIMM-SH7724

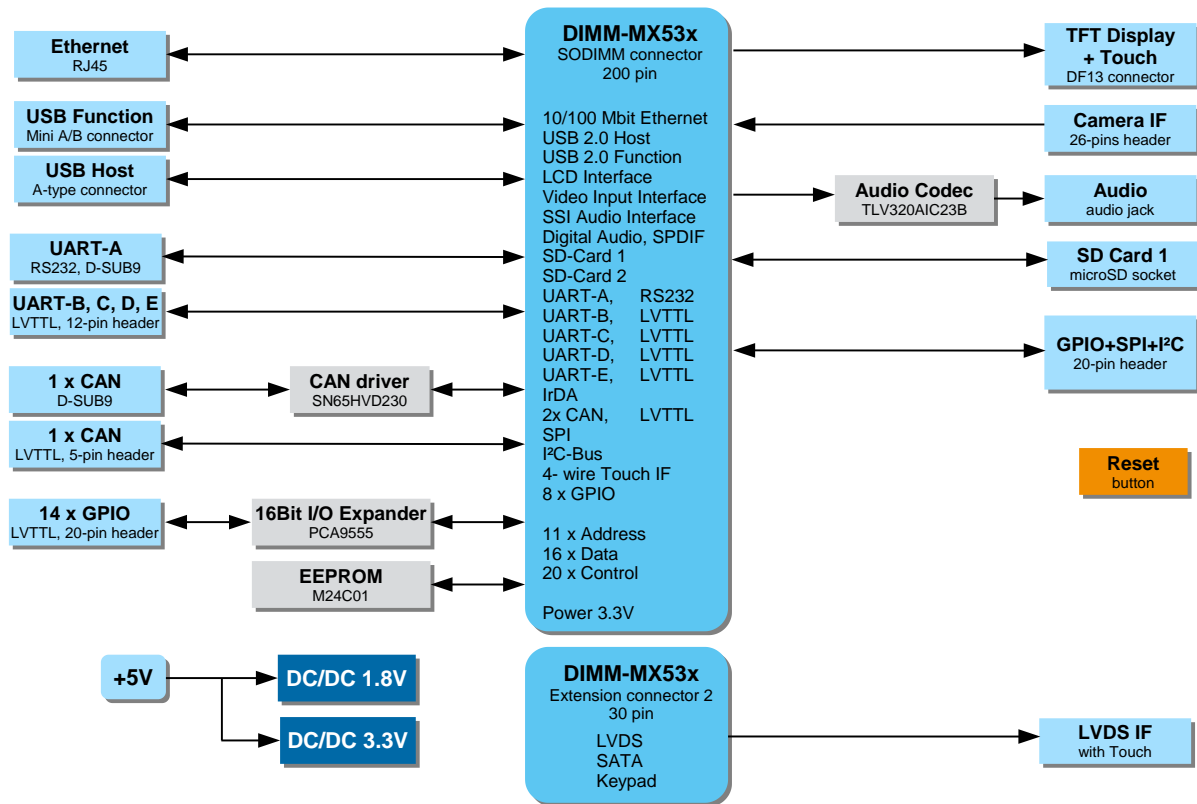


## 2.3 DIMM-MX257

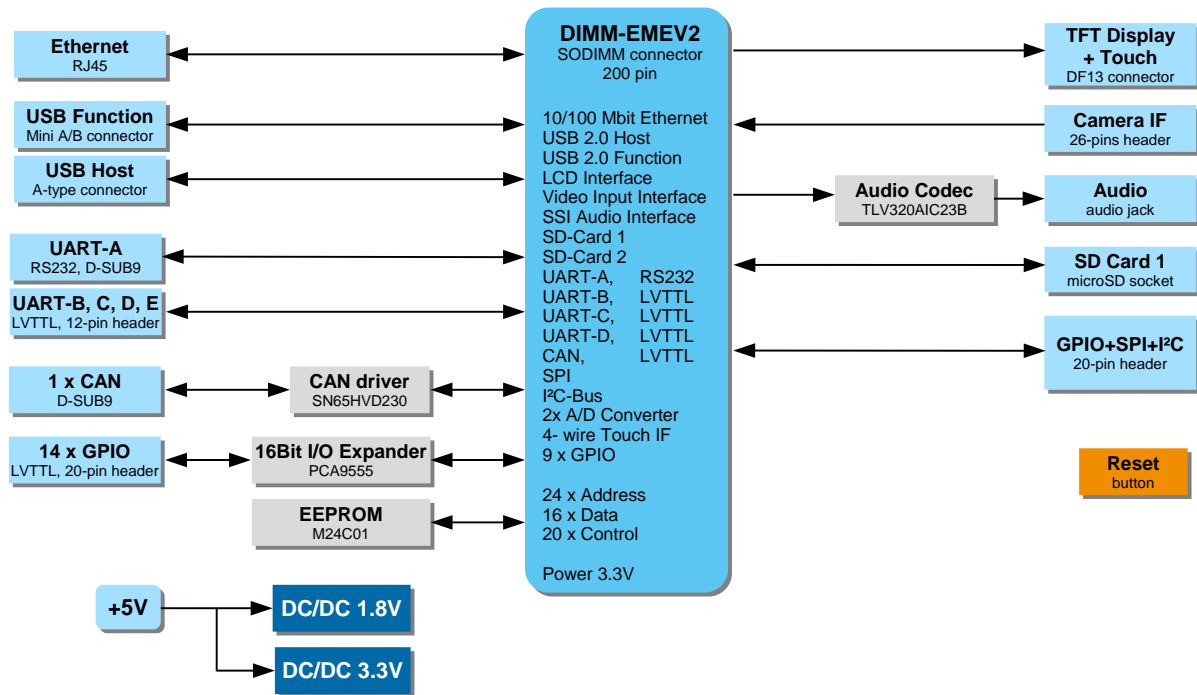




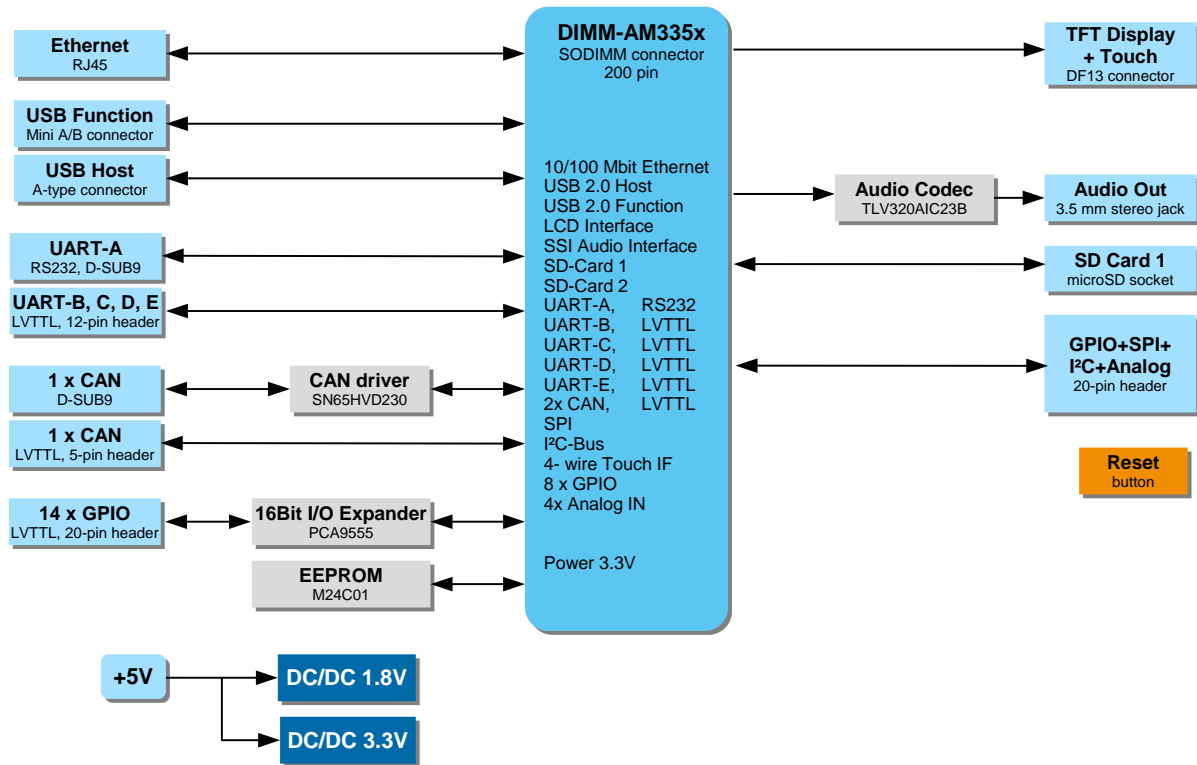
## 2.4 DIMM-MX53x



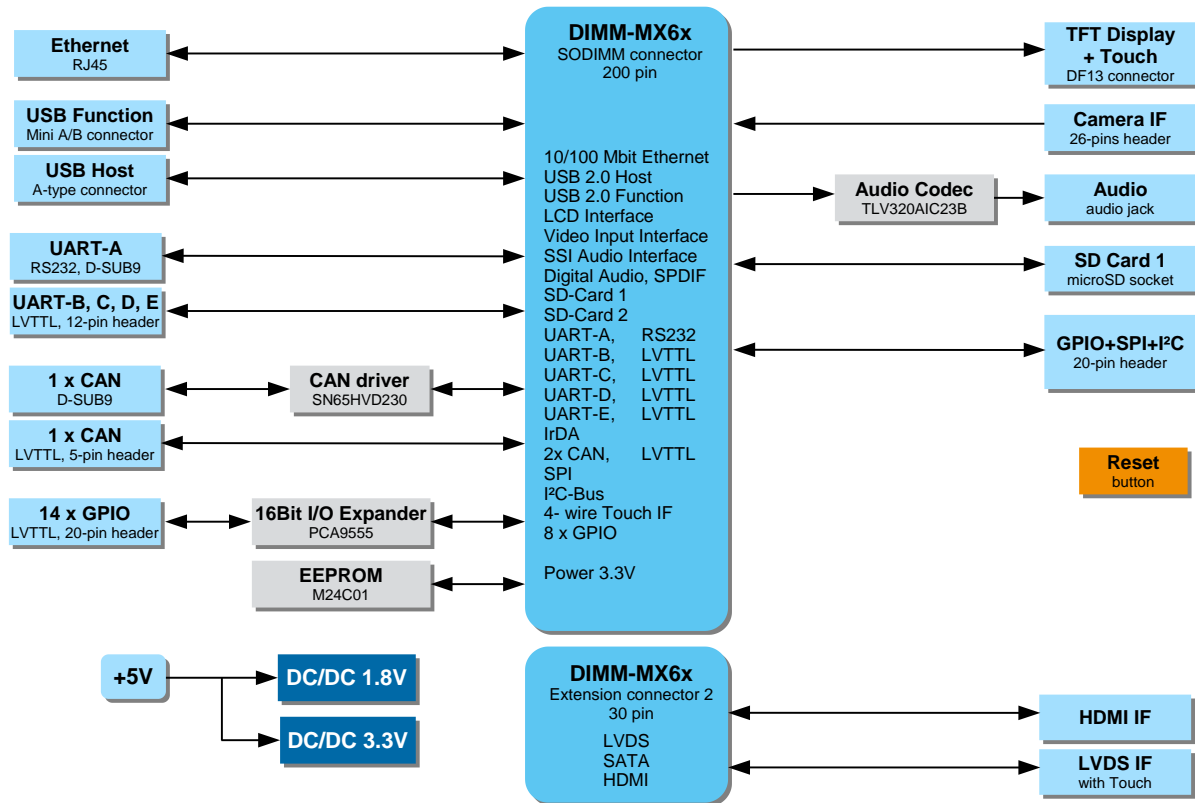
## 2.5 DIMM-EMEV2



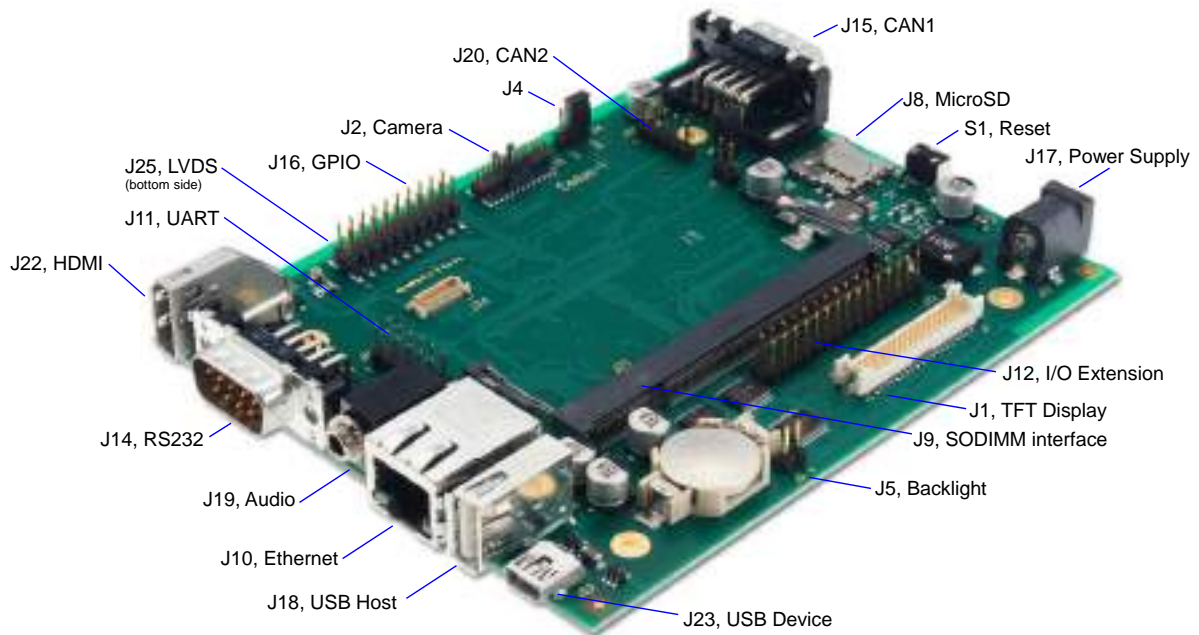
## 2.6 DIMM-AM335x



## 2.7 DIMM-MX6x



### 3 Connector Overview



### 4 Handling Precautions

Please read the following notes prior to installing CPU module to the Cadun base board. They apply to all ESD (electrostatic discharge) sensitive components:

- Before installing a CPU module the Cadun base board needs to be configured depending on the used CPU module. Further information can be found later in this document.
- Before touching the base board it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) a CPU module, unplug the power cable from your mains supply.
- Also switch off the power supply before plug or unplug cables at not ESD protected connectors.
- Handle the board with care and try to avoid touching its components or tracks.

## 5 First Configuration

Before installing a CPU module do the following configuration:

### 5.1 Ethernet

Because of different Ethernet Controllers the voltage for the LAN transformer must be configured depending on the used CPU module. This can be done with the jumper J<sub>4</sub> near the CAN connector.

The following table shows the jumper position:

CPU module	Position
DIMM-SH7723	1V8
DIMM-SH7724	3V3
DIMM-MX257	3V3
DIMM-MX53x	3V3
DIMM-EMEV2	1V8
DIMM_AM335x	3V3
DIMM-MX6x	3V3

## 6 Functional Description

### 6.1 List of features

The DIMM-Eco-Base Cadun provides the following interfaces and functions. Depending to the used CPU module there will be some differences which are described later in the document.

- 200 pin SODIMM connector for processor modules
- 10/100Base-Tx Ethernet interface at RJ45 jack
- 1 x USB 2.0 Device interface at Type-MINI A/B jack
- 1 x USB 2.0 Host interface at Type-A jack
- generic display interface for TFT displays with 18bpp including an interface for 4-wire resistive touch screens
- HDMI interface
- LVDS interface
- switched 5 Volt power source for display backlight
- 1 generic camera interface for CMOS cameras
- analog audio with stereo headphone output at 3.5mm audio jacks
- 1 micro SD-Card socket
- up to 5 serial ports, one as RS232 at D-SUB-9 jack, the other as LVTTL
- 1 CAN DSUB-9 connector, depending on the CPU module
- Connector for one CAN channel (LVTTL), depending on the CPU module
- 30 pin header for SPI, I2C, analog input and GPIOs
- 16-Bit I2C-I/O-Expander for 14 GPIO's
- I2C revision EEPROM
- Spread Spectrum Oscillator
- 1 reset button
- Battery holder for RTC backup, CR1632
- Power jack +5V

## 6.2 Features and specificities

Most of the features which are available with Cadun work as described on the Core module hardware documentation because the base board only provides the connectors.

Legend:

“Core”: feature from the Core module; please refer to the Cores hardware documentation to know how to use it.

“Base”: feature is specific to the Cadun base board; all information on how to use it are given in the present manual

“NA”: not applicable; this feature is not available with the specified Core module

Feature	DIMM-SH7723	DIMM-SH7724	DIMM-MX257	DIMM-MX53x	DIMM_EMEV2	DIMM-AM335x	DIMM-MX6x
Ethernet	Core	Core	Core	Core	Core	Core	Core
USB 2.0 Host	Core	Core	Core	Core	Core	Core	Core
USB 2.0 Device	Core	Core	Core <sup>5</sup>	Core <sup>5</sup>	Core	Core <sup>5</sup>	Core <sup>5</sup>
TFT Display (generic)	Core	Core	Core	Core	Core	Core	Core
HDMI	n/a	n/a	n/a	n/a	n/a	n/a	Core
LVDS	n/a	n/a	n/a	Core	n/a	n/a	Core
Touch Screen	Core	Core	Core	Core	Core	Core	Core
Camera Input	Core	Core	Optional <sup>1</sup>	Core	Core	n/a	Core
Analog Audio	Base	Base	Base	Base	Base	Base	Base
microSD-Card Socket	Core	Core	Core	Core	Core	Core	Core
UART (-A) RS232	Core	Core	Core	Core	Core	Core	Core
UART (-B, -C, -D, -E)	4 ports	3 ports	3 ports	4 ports	3 ports	3 ports	4 ports
LVTTTL	Core	Core	Core	Core	Core	Core	Core
IrDA	Core	Core	3 ports Core	4 ports Core	n/a	n/a	4 ports Core
CAN	n/a	1 port Core	1 port Core	1 port Core <sup>4</sup>	1 port Core	1 port Core	1 port Core
CAN (LVTTTL)	n/a	n/a	1 port Core	1 port Core	n/a	1 port Core	1 port Core
SPI	Core	Core	Core	Core	Core	Core	Core



I <sup>2</sup> C	Core	Core	Core	Core	Core	Core	Core
<b>GPIO</b>	14 + min. 4 GPIOs <sup>2</sup>	14 + 10 GPIOs <sup>2</sup>	14+ 6 GPIOs <sup>2</sup>	14+ 8 GPIOs <sup>2</sup>	14 + 9 GPIOs <sup>2</sup>	14+ 8 GPIOs <sup>2</sup>	14+ 8 GPIOs <sup>2</sup>
<b>Analog Inputs</b>	1 input Core	n/a	1 input Core	n/a	1 input Core	1 input Core	n/a
<b>Spread Spectrum oscillator</b>	Base <sup>3</sup>	Base <sup>3</sup>	n/a	Base <sup>3</sup>	Base <sup>3</sup>	n/a	Base <sup>3</sup>

1: Please ask emtrion for more information.

2: 14 GPIO's are realized on the base, via a GPIO Expander. The others are Core module dependent.

3: Spread spectrum oscillator is located on the base and clock signal is routed to the Core module.

4: CAN is only supported by the DIMM-MX537 and not by DIMM-MX535.

5: If needed an USB Host can be realized on that interface. Please contact emtrion for more information

### 6.3 DIMM interface, J9

The DIMM interface is a standardized interface between the DIMM CPU boards from emtrion and carrier boards. The interface consists of a 200 pin SODIMM connector with 2.5V keying which is commonly used for DDR1 memory modules [1].

All peripheral functions of the CPU boards and a memory bus interface are available at this connection. Also power is supplied via the SODIMM interface. Mechanical characteristics and a general pinout specification can be found later in this document. Individual differences of the CPU boards can be found in their appropriate manuals.

#### Watch:

The pin assignment is specific for the emtrion boards and must not be used for other boards.

### 6.4 Ethernet, J10

A 10/100 MBit TX Ethernet interface is available via the RJ45 jack J10. The jack has integrated magnetic whose DC level can be sourced by 1.8V or 3.3V. The supply voltage must be configured by the jumper J4 depending on the used CPU module:

CPU module	Voltage
DIMM-SH7723	1.8V
DIMM-SH7724	3.3V
DIMM-MX257	3.3V
DIMM-MX53x	3.3V
DIMM_EMEV2	1.8V
DIMM_AM335x	3.3V
DIMM-MX6x	3.3V

Two LEDs show the signal traffic (LINK\_LED#, green) and 100 MBit transfer speed (SPEED\_LED#, green).

### 6.5 USB Host, J18

The USB Host interface of the CPU board is connected to the USB Type-A connector J18. The used EMC filters are dimensioned for High Speed Mode with 480 MBaud.

The VBUS output of the USB Host connector is controlled by an USB power switch. It can provide up to 5W.

The USB power switch can be controlled by the CPU module by the signal *USBH\_PEN#*. Low switches the power on, a high (default) switch it off. An overcurrent is reported to the CPU by the signal *USBH\_OC#*. Low indicates an overcurrent. High indicates no overcurrent (default).

The USB data signals, the two control signals and the switched VBUS signal are routed to the SODIM connector. The VBUS signal to the SODIMM connector is not a power supply. The DIMM module has the possibility to check the availability of VBUS.

## 6.6 USB Device, J23

The USB device interface is available at the USB Mini A/B connector J23. The used EMC filters are dimensioned for High Speed Mode with 480 MBaud. All other characteristics depend on the CPU module. The USB data signals and the VBUS signal are routed to the SODIMM connector.

## 6.7 Graphic Output

The DIMM-Eco-Base Cadun base board supports a generic interface for TFT displays with RGB or 80-Series interface. If supported by the used core module also a HDMI and a LVDS interface is provided.

The LCD interface is limited to 18bpp color depth. Other parameters, like resolution or clocks, depend on the used CPU module.

The colour mapping depends on the CPU module and is described its manuals.

### 6.7.1 Generic Display Interface, J1

The display interface J1 is a generic DF13-40 type connector that includes all signals needed to connect TFT displays with 18 bit color depth. It also includes signals for a 4-wire touch screen interface and an I2C interface.

The touch signals are shared with the LVDS connector J25 and can used either by the LVDS interface or the TFT RGB interface. If used by both interfaces this will cause malfunctions of the touch interface.

Please ask emtrion to find out which displays are supported.

### 6.7.2 Backlight Supply, J5

The connector J5 is a 2 pin header which is intended to supply the power for the backlight of the connected generic TFT display. J5 is connected via a power switch to the +5V voltage. The power switch is controlled by the *LCD\_DON* signal at pin 72 of the SODIMM connector. A low (default) at *LCD\_DON* switch the voltage off, a high switch it on.

### 6.7.3 Spread Spectrum Oscillator

Normally the CPU clock is used as clock source for the LCD controller. But often displays have a big influence in EMC tests. Therefore a spread spectrum oscillator is provided on the Cadun board. A spread spectrum oscillator spreads the clock frequency in a specific domain, resulting in a signal with a wider bandwidth.

As default the Cadun provides a 32MHz clock, which is spread by +/- 1,4%, at the SODIMM interface. The DIMM-SH7723, DIMM-SH7724 and DIMM-MX53x CPU modules can use this clock as external input for the LCD controller. At the DIMM-MX257 this function is not available. Please ask emtrion if other external clock frequencies are needed.

The switching between internal and external LCD clock can be done by software.

### 6.7.4 HDMI Interface

The HDMI signals of the extension connector J24 are routed to a HDMI connector to connecting standard PC monitors. The I<sup>2</sup>C bus (DDC) for display identification and the hot plug signal are adapted by a HDMI level shifter and ESD protection.

This feature is not supported by all of emtrions core modules!

### 6.7.5 Generic LVDS Interface

The LVDS connector J25 is a generic interface for LVDS signals to drive LVDS displays. Between the clock and the four data pairs the I<sup>2</sup>C bus and the signals for a resistive touch screen are available.

The connector also provides +3.3V and 5V (each 500mA max.).

The touch signals are shared with the generic TFT RGB connector J1 and can used either by the LVDS interface or the TFT RGB interface. If used by both interfaces this will cause malfunctions of the touch interface.

## 6.8 Camera Interface, J2

The VIO1 interface of the SODIMM interface can be used as a generic interface where a CMOS camera module can be connected.

The camera interface is routed as the generic interface to a 26 pin header J2 to connect CMOS camera modules. It includes the 4:2:2 YCbCr interface with data and control signals, the I<sup>2</sup>C-Bus, power down and reset signals and the supply voltages 3.3 V and 5 V.

As reset signal the global reset is used. If the used camera modules support the power down function, they can be powered down by the SODIMM signal *PWRDWN\_CAM*.

PWRDWN_CAM	Mode
0	Running (default)
1	Powered down

Please ask emtrion for details of supported CMOS camera modules.

## 6.9 Analog Audio

The DIMM-Eco-Base Cadun provides the high performance audio codec TLV320AIC23 [8]. The digital audio interface is connected to the SODIMM connector; the I<sup>2</sup>C-Bus (chip address 0x1B) is used for the control interface.

The codec provides a stereo headphone output (30mW into a 32 Ω load), at the 3.5mm audio jack J19.

## 6.10 MicroSD-Card Socket, J8

A microSD-Card socket J8 is available. All signals are directly connected to the SODIMM interface SDC1 without any further provisions. Thus the characteristics depend on the used CPU board. The write protect signal of the SDC1 interface is connected to GND, that the microSD-Card is never write protected.

## 6.11 CAN Interfaces

The DIMM-Eco-Base Cadun base board supports two CAN channels, because many of emtrion's CPU modules provide CAN controllers with up to two channels.

The following CPU modules supports CAN:

CPU module	CAN CH1	CAN CH2
DIMM-SH7723	n/a	n/a
DIMM-SH7724	Yes	n/a
DIMM-MX257	Yes	Yes
DIMM-MX537	Yes	Yes
DIMM-EMEV2	Yes	n/a
DIMM-AM335x	Yes	Yes
DIMM-MX6x	Yes	Yes

### 6.11.1 CAN 1 Interface, J15

The CAN channel 1 is routed to D-SUB connector J15. A high-speed CAN transceiver is realized on the base, so that the CAN interface can directly connected to a CAN network. If this interface is an endpoint a 120Ω resistor can be included by setting a jumper on connector J6.

### 6.11.2 CAN 2 Interface, J20

The transmit and receive signals of CAN channel 2 are routed together with 3.3V and GND to the pin header J20. The signals have LVTTTL level without a CAN transceiver.

Ask emtrion for an adapter with integrated transceiver and D-SUB connector for CAN channel 2.

## 6.12 Serial Ports

The DIMM-Eco-Base Cadun base board supports up to 5 serial ports, depending on the used CPU module. The ports are named UART\_A to UART\_E.

UART\_A is available at the D-SUB jack J14 as standard RS232 interfaces. UART\_B, UART\_C, UART\_D and UART\_E are connected with LVTTTL level to the pin header J11. The LVTTTL signals can be adapted to the customer's needs by adding the appropriate signal drivers (e.g. RS232, RS548, RS422 etc.). By using the adapter cable ADA\_RS232 from emtrion the LVTTTL signals also can be used as RS232 interface.

### DIMM-SH7723:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	SCIF3	RS232 transceiver on CPU module
UART_B	LVTTTL	-	SCIF5	
UART_C	LVTTTL	-	SCIF4	
UART_D	LVTTTL	-	SCIF2	
UART_E	LVTTTL	-	SCIF1	

#### DIMM-SH7724:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	SCIF3	RS232 transceiver on CPU module
UART_B	LVTTTL	-	SCIF4	optional
(UART_C)	LVTTTL	-	SCIF5	
UART_D	LVTTTL	-	SCIF2	
UART_E	LVTTTL	-	SCIF0	

#### DIMM-MX257:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART1	RS232 transceiver on CPU module
UART_B	LVTTTL	-	UART3	
UART_D	LVTTTL	-	UART5	
UART_E	LVTTTL	-	UART2	

#### DIMM-MX53x:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART1	RS232 transceiver on CPU module
UART_B	LVTTTL	-	UART3	
UART_C	LVTTTL	-	UART4	
UART_D	LVTTTL	-	UART5	
UART_E	LVTTTL	-	UART2	

#### DIMM-EMEV2:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART0	RS232 transceiver on CPU module
UART_B	LVTTTL	-	UART1	
UART_C	LVTTTL	-	UART2	
UART_D	LVTTTL	-	UART3	

#### DIMM-AM335x:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART0	RS232 transceiver on CPU module
UART_B	LVTTTL	-	UART1	
UART_C	LVTTTL	-	UART4	
UART_D	LVTTTL	-	UART3	
UART_E	LVTTTL	RTS, CTS	UART3	

#### DIMM-MX6x:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART2	RS232 transceiver on CPU module
UART_B	LVTTTL	-	UART1	
UART_C	LVTTTL	-	UART3	
UART_D	LVTTTL	-	UART4	
UART_E	LVTTTL	-	UART5	

### 6.13 IrDA Ports

Each UART LVTTTL port of DIMM-MX257, DIMM-MX53x and DIMM-MX6x can also be used as low speed Infrared port (IrDA v1.0). The IrDA ports are available on the pin header J11, if the port is not used as UART port. The UART and IrDA ports use the same transmit and receive signals.

#### DIMM-MX257:

Port	Level	CPU-IF
UART_B	LVTTTL	IrDA3
UART_D	LVTTTL	IrDA5
UART_E	LVTTTL	IrDA2

#### DIMM-MX53x:

Port	Level	CPU-IF
UART_B	LVTTTL	IrDA3
UART_C	LVTTTL	IrDA4
UART_D	LVTTTL	IrDA5
UART_E	LVTTTL	IrDA2

#### DIMM-MX6x:

Port	Level	CPU-IF
UART_B	LVTTTL	IrDA1
UART_C	LVTTTL	IrDA3
UART_D	LVTTTL	IrDA4
UART_E	LVTTTL	IrDA5

The DIMM-SH7723 and the DIMM-SH7724 support IrDA v1.2a. The IrDA signals of these modules use the SODIMM GPIO pins GPIO\_8 (RXD) and GPIO\_9 (TXD).

### 6.14 I/O Extension, J12

The 22 pin header J12 includes up to 10 GPIOs, one SPI interface and an I<sup>2</sup>C-Bus interface. The I<sup>2</sup>C-Bus interface is decoupled to the onboard bus devices via a repeater circuit. The signals are directly connected with the SODIMM connector. Their individual characteristics depend on the used CPU board. See the connector description later in this manual.

### 6.15 I<sup>2</sup>C Bus

At the DIMM-Eco-Base Cadun are several I<sup>2</sup>C-Bus clients:

Device	Slave	Chip Address (7Bit)
Audio Codec	TLV320AIC23	0x1B
16Bit I/O-Expander	PCA9555	0x26
EEPROM board revision	24LC01B	0x51
Generic LCD Interface	PCA8574APW	0x3A
	PCA9530	0x60
Camera Interface	CAM-IF	Depends on used camera

Further addresses are allocated by I<sup>2</sup>C devices used at the CPU modules. Please refer to the hardware manual of the used CPU module.

### 6.16 I<sup>2</sup>C Revision EEPROM

The CPU module can detect the type and revision of the base board by reading an EEPROM connected to the I<sup>2</sup>C bus. The 7-Bit address is 0x51. The write protection of the EEPROM is controlled by the jumper J7. If the jumper is not plugged the EEPROM is write protected. If the jumper is plugged, the EEPROM is no write protected.

The DIMM-ECOBBase Cadun baseboard code is 0xC5.

### 6.17 I<sup>2</sup>C GPIO Extension, J16

A 16bit I<sup>2</sup>C GPIO expander is connected to the I<sup>2</sup>C bus. The 7-Bit address is 0x26. 14 GPIO's (Port0[7:0] and Port1[5:0]) are routed to the GPIO connector J16. The GPIO's can assert an interrupt via the signal GPIO\_IRQ#. 2 expander ports (Port1[7:6]) are used for Cadun internal function.

Port1[7]; 12MHz clock disable:

This signal can disable the 12MHz audio clock. If this signal is low the 12MHz is disabled, if high (default) it is enabled.

Port1[6]; USBOTG Host Select:

If the USB Mini A/B connector shall be used as a USB Host or OTG interface the USB Host control signals (Power Enable, ID, overcurrent) are multiplexed to the SODIMM GPIO's GPIO<sub>1</sub>, GPIO<sub>2</sub> and GPIO<sub>3</sub>. If that signal is low, the USB Host control signals are routed to the SODIMM GPIO pins. If it is high (default) the GPIO's of the extension connector J12 are routed to the SODIMM GPIO pins.

### 6.18 Analog Input

Depending on the CPU module an analog input is available on the I/O extension connector J12. Their individual characteristics depend on the used CPU board. A 100 Ohm series resistor is implemented in the analog input signal.

### 6.19 Reset Button, S1

A reset button S1 is placed at the right side of the DIMM-Eco-Base Cadun. A reset of the CPU module (e.g. by a software reset) also resets the Cadun base board.

A reset is only asserted if the reset button is pressed longer than 3 seconds. Immediately after pressing the button an interrupt (POWER\_IRQ) is asserted and the operating system has the option to close the filesystem if necessary before the HW reset asserts.



## 6.20 Power Supply

The Cadun base board must be supplied by a +5Volt, +/- 5%, max. 5 A, wall adapter.

On the Cadun there are two 3.3V power rails. The primary 3.3V power rail is routed from the 3.3V DCDC converter to the SODIMM connector. Via the SODIMM signal POWER\_BASE\_ON the secondary 3.3V power rail is switch on. The Cadun interface components are connected to the secondary 3.3V power rail. They are only supplied, if the CPU module allows it.

This feature is realized to avoid latch up effects at power up and power down.

### 6.20.1 Onboard Regulators

The DIMM-Eco-Base Cadun has a switching regulator +3,3V (most of the base board functions and the CPU module) and a linear regulator for +1,8V (Ethernet).

The 3,3V regulator has a green LED to show the status of the voltage on the board. If the LED is on, the voltage is good.

### 6.20.2 Power Consumption

The maximum available power for the complete system must not exceed 25W!

#### **Important note:**

Please make sure your connected devices like display, USB devices, cameras etc. including the Cadun base board and the CPU module don't exceed the **25 Watt** limit! Otherwise this can damage your system!

## 6.21 Backup Battery

A battery holder J13 for lithium coin cell CR1632 is available to supply the RTC of the CPU boards.

## 7 Pin Assignments

### 7.1 J<sub>9</sub>, SODIMM connector

Type 200 pin SODIMM socket, 0.6 mm Pitch, 2,5V keying

Pin	Signal	Interface		Signal	Pin	
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2	
3	ETH_TDP			USBH_OC#	4	
5	ETH_TDM			USBH_DM	6	
7	GND			USBH_DP	8	
9	ETH_RDP			USB Device	USBF_VBUS	10
11	ETH_RDM				USBF_DM	12
13	LINK_LED#		USBF_DP		14	
15	USBH_VBUS <sup>1</sup>		USB Host	Power	GND	16
17	CAN <sub>1</sub> _TX		CAN	UART-A	UART_A_TXD#	18
19	CAN <sub>1</sub> _RX	UART_A_RXD#			20	
21	UART_E_TXD	UART-E	UART_A_RTS#		22	
23	UART_E_RXD		UART_A_CTS#		24	
25	UART_D_TXD	UART-D	Touch		Touch_XP	26
27	UART_D_RXD			Touch_XM	28	
29	UART_C_TXD	UART-C		Touch_YP	30	
31	UART_C_RXD			Touch_YM	32	
33	UART_B_TXD	UART-B	A/D	ANA <sub>1</sub>	34	
35	UART_B_RXD			n/c	36	
37	n/c	A/D		n/c	38	
39	+3V <sub>3</sub>	Power		GND	40	
41	n/c	LCD		n/c	42	
43	n/c			n/c	44	
45	n/c			n/c	46	
47	LCD_D <sub>16</sub>			LCD_D <sub>17</sub>	48	
49	LCD_D <sub>14</sub>			LCD_D <sub>15</sub>	50	
51	LCD_D <sub>12</sub>			LCD_D <sub>13</sub>	52	

53	LCD_D10		LCD_D11	54			
55	LCD_D8		LCD_D9	56			
57	LCD_D6		LCD_D7	58			
59	LCD_D4		LCD_D5	60			
61	LCD_D2		LCD_D3	62			
63	LCD_D0		LCD_D1	64			
65	+3V3	Power		GND	66		
67	LCDRD#	LCD		LCD_LCLK	68		
69	LCD_DISP			LCD_DCK	70		
71	LCD_HSYN			LCD_DON	72		
73	LCD_VSYN			LCD_VCPWC	74		
75	n/c			LCD_VEPWC	76		
77	n/c	VIO		CAM_D7	78		
79	n/c			CAM_D6	80		
81	n/c			CAM_D5	82		
83	CAM_CLK			CAM_D4	84		
85	CAM_HD			CAM_D3	86		
87	CAM_VD			CAM_D2	88		
89	PWRDWN_CAM		CAM_D1	90			
91	n/c		CAM_D0	92			
93	+3V3	Power		GND	94		
95	SPI2_MISO <sup>2</sup>	SDC2		SDC1_D0	96		
97	n/c			SDC1		SDC1_D1	98
99	n/c					SDC1_D2	100
101	SPI2_SS# <sup>2</sup>					SDC1_D3	102
103	SPI2_MOSI <sup>2</sup>					SDC1_CMD	104
105	SPI2_CLK <sup>2</sup>					SDC1_CLK	106
107	n/c					SDC1_CD#	108
109	n/c	SDC1_WP# (GND)	110				
111	SPI1_SS#	SPI		SPI1_MISO	112		
113	SPI1_SCK			SPI1_MOSI	114		

115	SCL	I2C	Audio	AUDIO_BCK	116
117	SDA			AUDIO_LRC	118
119	n/c			AUDIO_DATI	120
121	n/c	AUDIO_DATO		122	
123	GND	Power	AUDIO_MCLK	124	
125	GPIO8/CAN2_RX	GPIO	GPIO9/CAN2_TX	126	
127	GPIO6		GPIO7	128	
129	GPIO4		GPIO5	130	
131	GPIO2		GPIO3	132	
133	GPIO0		GPIO1	134	
135	POWER_ON_BASE	Power	GND	136	
137	n/c	Address A[15:0]	n/c	138	
139	n/c		n/c	140	
141	n/c		n/c	142	
143	n/c		n/c	144	
145	n/c		n/c	146	
147	n/c		n/c	148	
149	n/c		n/c	150	
151	n/c		n/c	152	
153	n/c		n/c	154	
155	n/c		n/c	156	
157	n/c		n/c	158	
159	n/c		n/c	160	
161	+3V3	Power	GND	162	
163	n/c	Data D[15:0]	n/c	164	
165	n/c		n/c	166	
167	n/c		n/c	168	
169	n/c		n/c	170	
171	n/c		n/c	172	
173	n/c		n/c	174	
175	n/c		n/c	176	

177	n/c	<b>Bus Control</b>	n/c	178	
179	n/c		n/c	180	
181	n/c		n/c	182	
183	n/c		GPIO_IRQ	184	
185	n/c		POWER_IRQ	186	
187	n/c		CAP_TOUCH_IRQ#	188	
189	n/c		RESO#	190	
191	n/c		RESI#	192	
193	n/c		n/c	194	
195	n/c		n/c	196	
197	n/c		n/c	198	
199	BAT		<b>Power</b>	GND	200

- 1: USBH\_VBUS is generated on the Base and it is routed to the Core module that it can be monitored.
- 2: The DIMM-7724 has routed a second SPI interface to the SDC2 pins of the SODIMM interface.

## 7.2 J1, Generic TFT Connector

Type: 40 pin connector, Hirose DF13-40, 1.25 mm \* 1.25 mm pitch

Pin	Signal	Pin	Signal
1	LCD VEPWC	2	LCD VCPWC
3	SDA	4	SCL
5	LCDRD#	6	CAP_TOUCH_IRQ#
7	TFT_VCC	8	TFT_VCC
9	DE	10	GND
11	BLUE5	12	BLUE4
13	BLUE3	14	BLUE2
15	BLUE1	16	BLUE0
17	GND	18	GREEN5
19	GREEN4	20	GREEN3
21	GREEN2	22	GREEN1
23	GREEN0	24	GND
25	RED5	26	RED4
27	RED3	28	RED2
29	RED1	30	RED0
31	GND	32	VSYNC
33	HSYNC	34	DOTCLK
35	GND	36	TFT_VCC
37	Touch_XP	38	Touch_YP
39	Touch_XM	40	Touch_YM

### 7.3 J22, HDMI Connector

Type: HDMI connector, Tyco 2007435-1

Pin	Signal	Pin	Signal
1	HDMI_D2_P	2	GND
3	HDMI_D2_N	4	HDMI_D1_P
5	GND	6	HDMI_D1_N
7	HDMI_Do_P	8	GND
9	HDMI_Do_N	10	HDMI_CLK_P
11	GND	12	HDMI_CLK_N
13	HDMI_CEC_OUT	14	n/c
15	HDMI_I2C_SCL	16	HDMI_I2C_SDA
17	GND	18	HDMI_5V
19	HDMI_HPD	<b>SHIELD</b>	GND

### 7.4 J25, Generic LVDS Connector

Type: 25 pin connector, JAE FI-S25P-HFE, 1,25mm pitch

Pin	Signal	Pin	Signal
1	+3.3V (500mA max.)	2	+3.3V
3	SCL	4	SDA
5	GND	6	LVDS_TX2_N
7	LVDS_TX2_P	8	GND
9	LVDS_TX0_N	10	LVDS_TX0_P
11	GND	12	LVDS_TX1_N
13	LVDS_TX1_P	14	GND
15	LVDS_CLK_N	16	LVDS_CLK_P
17	GND	18	LVDS_TX3_N
19	LVDS_TX3_P	20	GND
21	TOUCH_XP	22	TOUCH_XM
23	TOUCH_YP	24	TOUCH_YM
25	+5V (500mA max.)		

### 7.5 J5, Backlight Power Supply

Type: 2 pin header, 2.54 mm pitch

Pin	Signal
1	+5V
2	GND

### 7.6 J14, UART-A

Type: DSUB-9 male

Pin	Signal	Pin	Signal
1	n/c	6	n/c
2	UART_A_RXD#	7	UART_A_RTS#
3	UART_A_TXD#	8	UART_A_CTS#
4	n/c	9	n/c
5	GND		

### 7.7 J11, UART-B, C, D, E

Type: 2\*6 pin header, 2.54 mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	UART_B_RXD*
3	GND	4	UART_B_TXD*
5	UART_E_TXD	6	UART_C_RXD*
7	UART_E_RXD	8	UART_C_TXD*
9	UART_D_TXD	10	GND
11	UART_D_RXD	12	+3.3V



## 7.8 J2, Generic Camera Connector

Type: 2\*13 pin header, 1.27 mm pitch

Pin	Signal	Pin	Signal
1	n/c	2	GND
3	+5V	4	GND
5	CAM_Do	6	CAM_D1
7	CAM_D2	8	CAM_D3
9	CAM_D4	10	CAM_D5
11	CAM_D6	12	CAM_D7
13	GND	14	GND
15	CAM_VD	16	PWRDOWN_CAM#
17	CAM_HD	18	GND
19	CAM_CLK	20	RESO#
21	+3.3V	22	GND
23	SCL	24	SDA
25	+3.3V	26	GND

## 7.9 J15, CAN connector

Type: DSUB-9 male

Pin	Signal	Pin	Signal
1	n/c	6	n/c
2	CAN1_L	7	CAN1_H
3	GND	8	n/c
4	n/c	9	n/c
5	n/c		

### 7.10 J20, CAN LVTTTL connector

Type: 1\*5 pin header, 2.54 mm pitch

Pin	Signal
1	+3.3V
2	GND
3	CAN2_TX
4	CAN2_RX
5	n/c

### 7.11 J8, microSD Socket

Type: microSD Socket, 14 Pin

Pin	Signal
1	SDC1_D2
2	SDC1_D3
3	SDC1_CMD
4	3V3
5	SDC1_CLK
6	GND
7	SDC1_Do
8	SDC1_D1
9	SDC1_CD#
10	GND
11	GND
12	GND
13	GND
14	GND

## 7.12 J12, I/O Extension Connector

Type: 2\*15 pin header, 2.54 mm pitch

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	SPI1_SS#	4	GPIO_0
5	SPI1_SCK	6	GPIO_1
7	SPI1_MISO	8	GPIO_2
9	SPI1_MOSI	10	GPIO_3
11	GND	12	GPIO_4
13	SPI2_SS#	14	GPIO_5
15	SPI2_SCK	16	GPIO_6
17	SPI2_MISO	18	GPIO_7
19	SPI2_MOSI	20	GPIO_8
21	GND	22	GPIO_9
23	SCL	24	RESO#
25	SDA	26	RESI#
27	GND	28	+3.3V
29	ANA1	30	+3.3V

### 7.13 J16, GPIO Expander Connector

Type: 2\*10 pin header, 2.54 mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	GND
3	GPIO_I2C_0	4	GPIO_I2C_8
5	GPIO_I2C_1	6	GPIO_I2C_9
7	GPIO_I2C_2	8	GPIO_I2C_10
9	GPIO_I2C_3	10	GPIO_I2C_11
11	GPIO_I2C_4	12	GPIO_I2C_12
13	GPIO_I2C_5	14	GPIO_I2C_13
15	GPIO_I2C_6	16	n/c
17	GPIO_I2C_7	18	n/c
19	GND	20	+3.3V

### 7.14 J10, Ethernet Connector

Type: Rj45 Jack (8 pin)

Pin	Signal
1	ETH_TDP
2	ETH_TDM
3	ETH_RDP
4	n/c
5	n/c
6	ETH_RDM
7	n/c
8	n/c

### 7.15 J<sub>4</sub>, LAN transformer voltage connector

Type: 1\*3 pin header, 2.54 mm pitch

Pin	Signal
1	+3.3V
2	LAN_voltage
3	+1.8V

### 7.16 J<sub>18</sub>, USB Host Connector

Type: USB A connector (4 pin)

Pin	Signal
1	USBH_VBUS
2	USBH_DM
3	USBH_DP
4	GND

### 7.17 J<sub>23</sub>, USB Device Connector

Type: USB mini AB connector (5 pin)

Pin	Signal
1	USBF_VBUS
2	USBF_DM
3	USBF_DP
4	USB_ID
5	GND

### 7.18 J<sub>19</sub>, Audio Jack

Type: Audio Jack

Pin	Signal
1	LEFT
2	n/c
3	n/c
4	RIGHT

### 7.19 J23, RTC Battery Holder

Type: Battery Holder for CR1632

Pin	Signal
1	GND
2	BAT +

### 7.20 J17, DC Power Jack

Type: KLDX-SMT-0202AP

Pin	Signal
Center Pin	+5V
Outer Ring	GND

## 8 Technical Characteristics

### 8.1 Electrical Specifications

Electrical Specification	
Supply Voltage	+5V, +/-5%
Current consumption	max. 5A, depending on Core module an connected peripherals

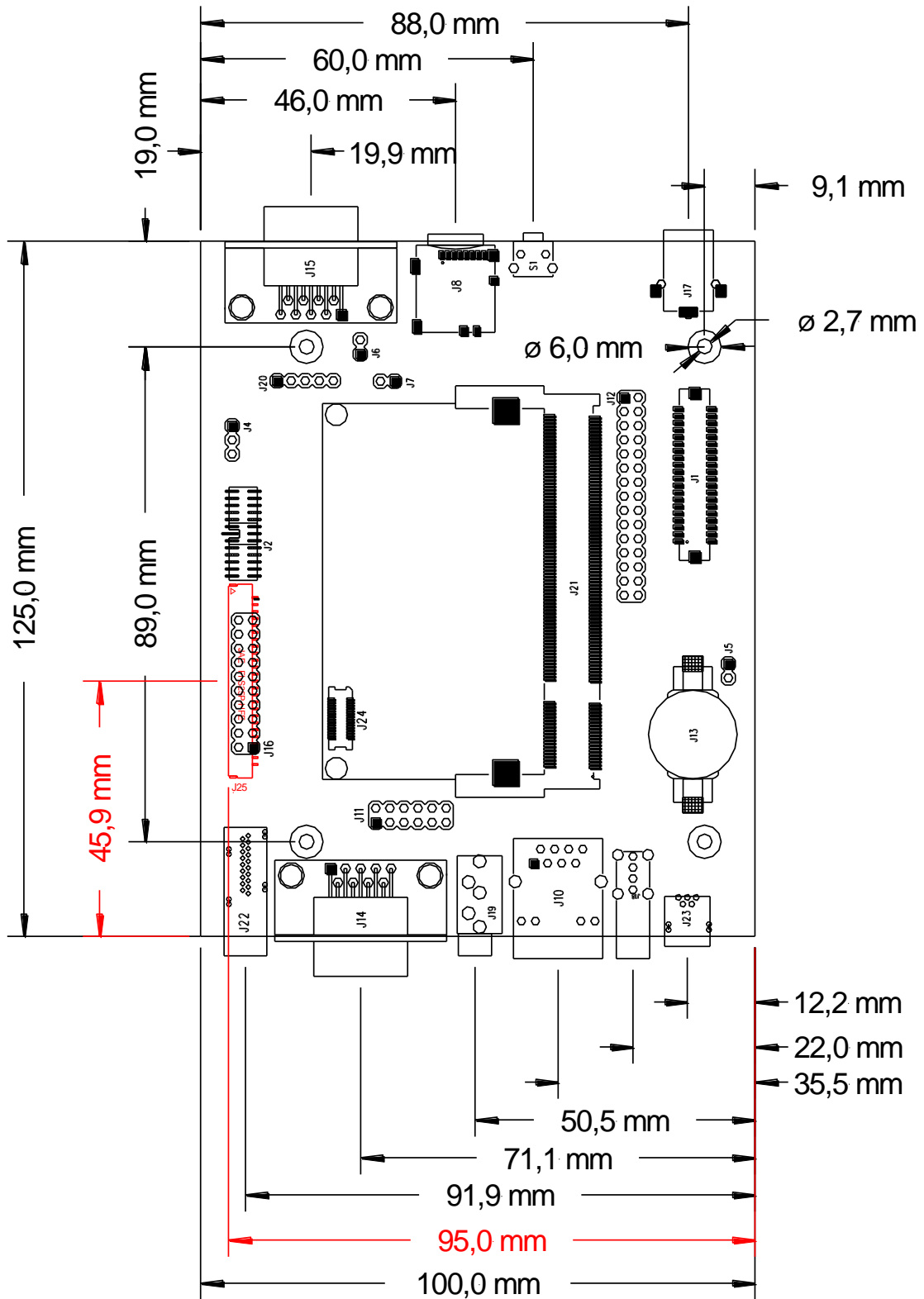
### 8.2 Environmental Specifications

Operating temperature	
Standard	-25°C ... +85°C
Storage temperature	
Storage temperature	-40 ... +125°C
Relative humidity	
Relative humidity	0 ... 95 %, non-condensing

### 8.3 Mechanical Specifications

Mechanical Specifications	
Weight	approx. 102 g
Board	Glasepoxi FR-4, UL-listed, 4 layers
Dimensions	125 mm x 100 mm x 18 mm

8.3.1 Dimensional Drawing





## 9 References

- [1] DDR1 & DDR2 SODIMM Socket 0.6 mm Pitch 200 Pos Standard Profile  
Standard Type  
Tyco Electronics  
Part Number: 1473005-1
  
- [2] TLV320AIC23B  
Stereo Audio CODEC, 8- to 96-kHz, With Integrated Headphone Amplifier  
February 2004  
Texas Instruments